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Simulation & Implementation Of Three Phase Induction Motor On Single Phase By Using PWM Techniques

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Abstract—The main objective of this paper is to control the speed of an induction motor by changing the frequency using three level diode clamped multilevel inverter. To obtain high quality sinusoidal output voltage with reduced harmonics distortion, multicarrier PWM control scheme is proposed for diode clamped multilevel inverter. This method is implemented by changing the supply voltage and frequency applied to the three phase induction motor at constant ratio. The proposed system is an effective replacement for the conventional method which produces high switching losses, results in poor drive performance. The simulation & implementation results reveal that the proposed circuit effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD). The effectiveness of the system is checked by simulation using MATLAB 7.8 simulink package.
Keywords— Clamped Diode, MOSFET, Induction motor, Multicarrier PWM technique, THD.

INTRODUCTION

Majority of industrial drives use ac induction motor because these motors are rugged, reliable, and relatively inexpensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable-frequency supply voltage [1]. But many applications need variable speed operations. Historically, mechanical gear systems were used to obtain variable speed. Recently, power electronics and control systems have matured to allow these components to be used for motor control in place of mechanical gears. These electronics not only control the motor's speed, but can improve the motor's dynamic and steady state characteristics. Adjustable speed ac machine system is equipped with an adjustable frequency drive that is a power electronic device for speed control of an electric machine. It controls the speed of the electric machine by converting the fixed voltage and frequency to adjustable values on the machine side. High power induction motor drives using classical three - phase converters have the disadvantages of poor voltage and current qualities. To improve these values, the switching frequency has to be raised which causes additional switching losses. Another possibility is to put a motor input filter
between the converter and motor, which causes additional weight. A further inconvenience is the limited voltage that can be applied to the induction motor determined by inconvenience is the limited voltage that can be applied to the induction motor determined by the blocking voltage of the semiconductor switches. The concept of multilevel inverter control has opened a new possibility that induction motors can be controlled to achieve dynamic performance equally as that of dc motors [2].

Recently many schemes have been developed to achieve multilevel voltage profile, particularly suitable for induction motor drive applications. The diode clamp method can be applied to higher level converters. As the number of level increases, the synthesized output waveform adds more steps, producing a staircase waveform. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels [3]. Unfortunately, the number of the achievable levels is quite limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout and packaging constraints. In this paper, a three-phase diode clamped multilevel inverter fed induction motor is described. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors [4]. The voltage across the switches has only half of the dc bus voltage. These features effectively double the power rating of voltage source inverter for a given semiconductor device [5]. The proposed inverter can reduce the harmonic contents by using multicarrier PWM technique. It generates motor currents of high quality. V/f is an efficient method for speed control in open loop. In this scheme, the speed of induction machine is controlled by the adjustable magnitude of stator voltages and its frequency in such a way that the air gap flux is always maintained at the desired value at the steady-state. Here the speed of an induction motor is precisely controlled by using three level diode clamped multilevel inverter.

CONVENTIONAL METHOD

The voltage source inverter produces an output voltage or a current with levels either zero or ±Vdc. They are known as two level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse-width modulation strategies. In high power and high-voltage applications, these two-level inverters have some limitations in operating at high frequency mainly due to switching losses and constraints of device rating. The dc link voltage of a two-level inverter is limited by voltage ratings of switching devices, the problematic series connection of

switching devices is required to raise the dc link voltage. By series connection, the maximum allowable switching frequency has to be more lowered; hence the harmonic reduction becomes more difficult [6]. In addition, the two level inverters generate high frequency common-mode voltage within the motor windings which may result in motor and drive application problems [7]. From the aspect of harmonic reduction and high dc-link voltage level, three-level approach seems to be the most promising alternative. The harmonic contents of a three-level inverter are less than that of a two-level inverter at the same switching frequency and the blocking voltage of the switching device is half of the dc-link voltage [8]. A three level inverter will not generate common-mode voltages when the inverter output voltages are limited within
certain of the available switching states [9]. So the three-level inverter topology is generally used in realizing the high performance, high voltage ac drive systems [10].

DRIVE SYSYEM DESCRIPTION

In the conventional technique normal PWM method is used. So that the voltage and current is of poor qualities and the switching frequency causes more amount of switching losses. Those drawbacks are rectified using three phase diode clamped multilevel inverter. The voltage and current quality are better and the switching losses are reduced when compared to the conventional technique. Also the THD is found to be better.

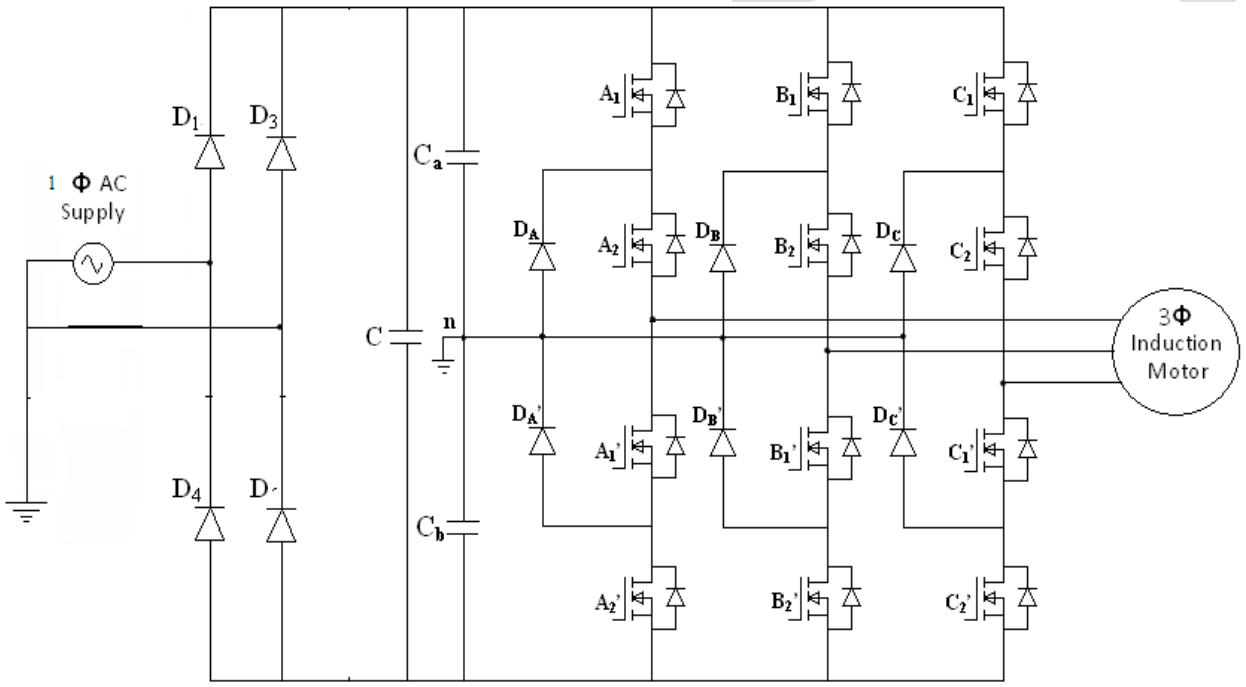


Fig. 2. Multilevel inverter based drive circuit

Structure of Three Level Diode Clamped Multilevel Inverter

The three-level neutral point-clamped voltage source inverter is shown in Fig.2. It contains 12 unidirectional active switches and 6 neutral point clamping diodes. The middle point of the two capacitors "*n"* can be defined as the neutral point [7]. The major benefit of this configuration is each switch must block only one-half of the dc link voltage (Vdc/2). In order to produce three levels, only two of the four switches in each phase leg should be turned on at any time. The dc-bus voltage is split into three levels by two series-connected bulk capacitors, Ca and Cb, they are same in rating. The diodes are all same type to provide equal voltage sharing and to clamp the same voltage level across the switch, when the switch is in off condition. Hence this structure provides less voltage stress across the switch.

PRINCIPLE OF OPERATION

To produce a staircase-output voltage, consider one leg of the three-level inverter, as shown in Fig.3. The steps to synthesize the three-level voltages are as follows.
1. For an output voltage level Vao=Vdc, turn on all upper-half switches A1 and A2.
2. For an output voltage level Vao=Vdc, turn on one upper switch A2 and one lower switch A1'.

3. For an output voltage level Vao=0, turn on all lower half switches A1' and A2'.

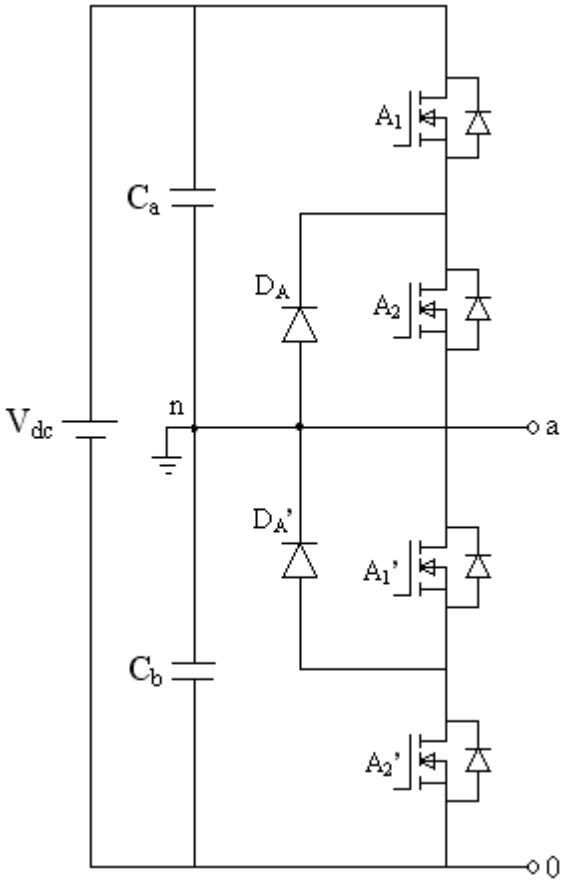


Fig.3. One leg of a bridge.

Table.1. shows the voltage levels and their corresponding switch states. State condition 1 means the switch is on, 0 means the switch is off. There are two complementary switch pairs in each phase. These pairs for one leg of the inverter are (A1, A1'), (A2, A2'). If one of the complementary switch pairs is turned on, the other of the same pair must be off.

Output V_{ao}	Switch State			
	A_1	A_1'	A_2	A_2'
V_{dc}	1	1	0	0
$V_{dc}/2$	0	1	1	0
0	0	0	1	1

TABLE 1 Output voltage levels and their Switching states.

Fig.4. shows the phase voltage waveform of the three-level inverter. The m-level converter has an m-level output phase-leg voltage and a (2m-1)-level output line voltage.

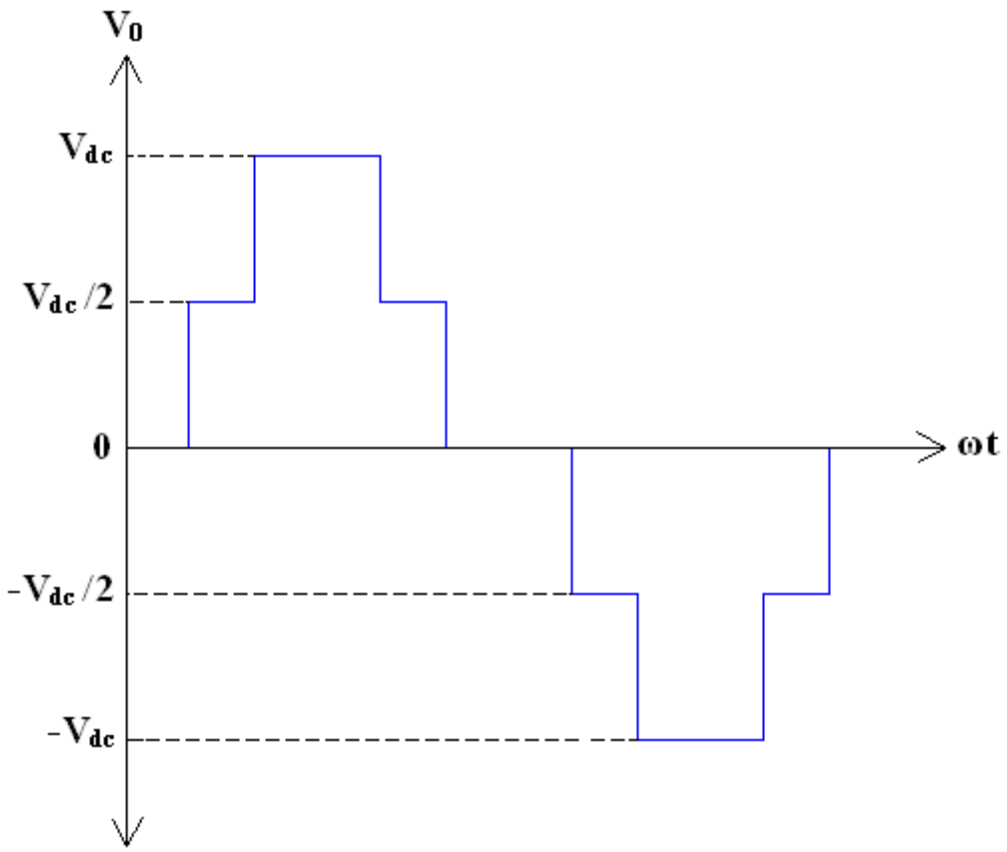


Fig.4. Three level inverter output voltage.

The most attractive features of multilevel inverters are as follows.

- They can generate output voltages with extremely low distortion and lower dv/dt.
- They draw input current with very low distortion [7].
- They generate smaller common mode (CM) voltage, thus reducing the stress in the motor bearings.
- They can operate with a lower switching frequency [7].

PROPOSED SCHEME

The block schematic of multilevel inverter fed three phase induction motor is as shown in Fig.5. The complete system will consist of two sections; a power circuit and a control circuit. The power section consists of a power rectifier, filter capacitor, and three phase diode clamped multilevel inverter. The motor is connected to the multilevel inverter.

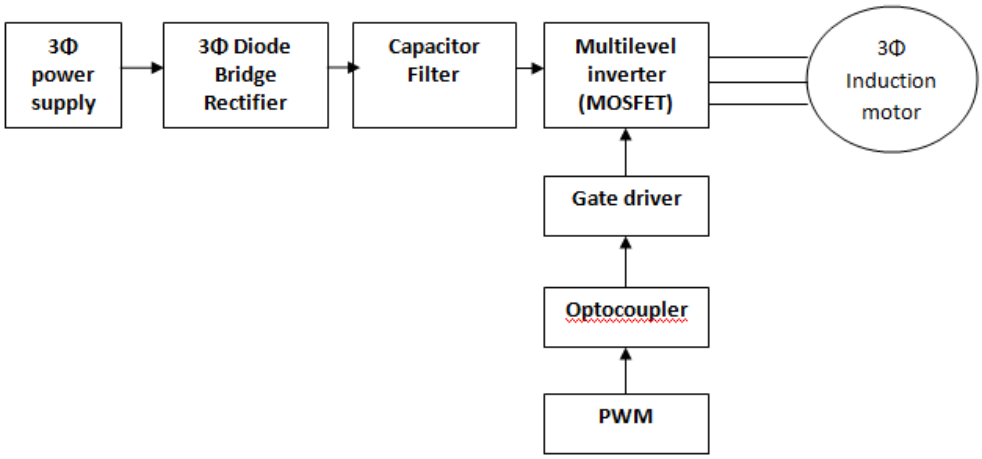


Fig.5. Basic block diagram.

The complete system will consist of two sections; a power circuit and a control circuit. The power section consists of a power rectifier, filter capacitor, and three phase diode clamped multilevel inverter. The motor is connected to the multilevel inverter. Fig.6 shows an ac input voltage is fed to a three phase diode bridge rectifier with capacitor filter. A capacitor filter, removes the ripple contents present in the dc output voltage.

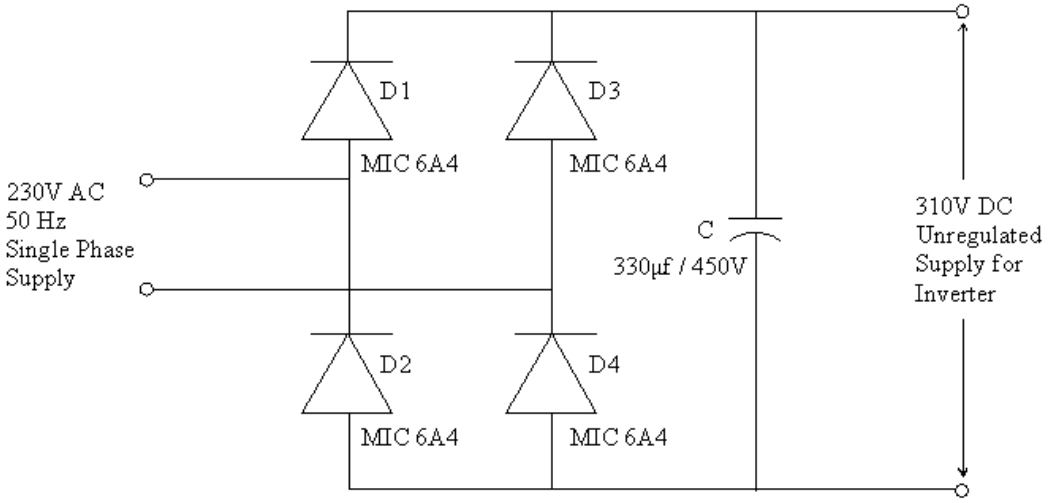


Fig.6 Ac input voltage is fed to a three phase diode bridge rectifier with capacitor filter

The pure dc voltage is applied to the three phase multilevel inverter through capacitor filter. The multilevel inverter has 12 MOSFET switches that are controlled in order to generate an ac output voltage from the dc input voltage. The control circuit of the proposed system consists of three blocks namely PWM opto-coupler and gate driver circuit. Fig.7. Shows circuit diagram of PWM

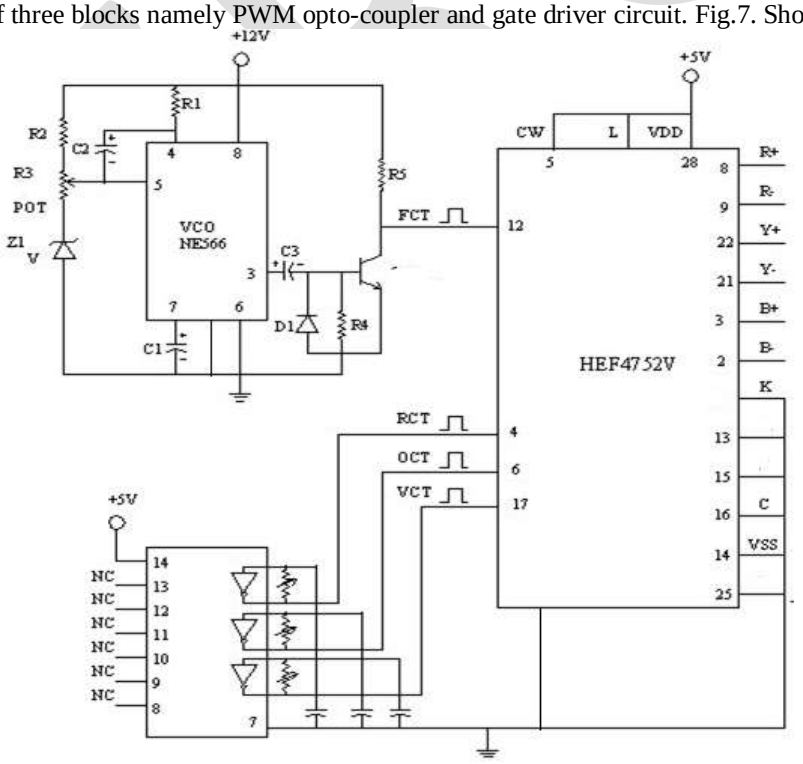


Fig.7 Circuit for PWM

The PWM is used four clocks reference clock, voltage control clock, frequency clock, output delay clock. For this clock we used the VCO which generate frequency clock & Schmitt trigger which used for generating the reference clock, output delay clock,

voltage control clock. The PWM is used for generating gating signals required to drive the power MOSFET switches present in the multilevel inverter. The voltage magnitude of the gate pulses generated by the PWM is normally 5V. To drive the power switches satisfactorily the opto-coupler and driver circuit are necessary in between the controller and multilevel inverter. The output ac voltage is obtained from the multilevel inverter can be controlled in both magnitude and frequency (V/f open loop control). The controlled ac output voltage is fed to the induction motor drive. When the power switches are on, current flows from the dc bus to the motor winding. The motor windings are highly inductive in nature; they hold electric energy in the form of current. This current needs to be dissipated while switches are off. Diodes are connected across the switches give a path for the current to dissipate when the switches are off. These diodes are also called freewheeling diodes. The V/f control method permits the user to control the speed of an induction motor at different rates. For continuously variable speed operation, the output frequency of multilevel inverter must be varied. The applied voltage to the motor must also be varied in linear proportion to the supply frequency to maintain constant motor flux.

MODULATION STRATEGY

This Paper mainly focuses on multicarrier PWM method. This method is simple and more flexible than SVM methods. The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. If an n-level inverter is employed, n-1 carriers will be needed. The carriers have the same frequency WC and the same peak to peak amplitude Ac and are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency Wm and amplitude Am. At every instant each carrier is compared with the modulating signal. Each comparison gives 1(-1) if the modulating signal is greater than (lower than) the triangular carrier in the first (second) half of the fundamental period, 0 otherwise. The results are added to give the voltage level, which is required at the output terminal of the inverter. Multicarrier PWM method can be categorized into two groups: 1) Carrier Disposition (CD) method 2) Phase shifted PWM method.

Advantages of multicarrier PWM techniques:

- Easily extensible to high number of levels.
- Easy to implement.
- To distribute the switching signals correctly in order to minimize the switching losses.
- To compensate unbalanced dc sources.

Related to the way the carrier waves are placed in relation to the reference signal, three cases can be distinguished:

- Alternative Phase Opposition Disposition (APOD), where each carrier band is shifted by 180° from the adjacent bands.
- Phase Opposition Disposition (POD), where the carriers above the zero reference are in phase, but shifted by 180° from those carriers below the zero reference.
- In-Phase Disposition (PD), where all the carriers are in phase [8].

In this paper the gating pulses for MOSFET switches are generated by using In-phase disposition technique.

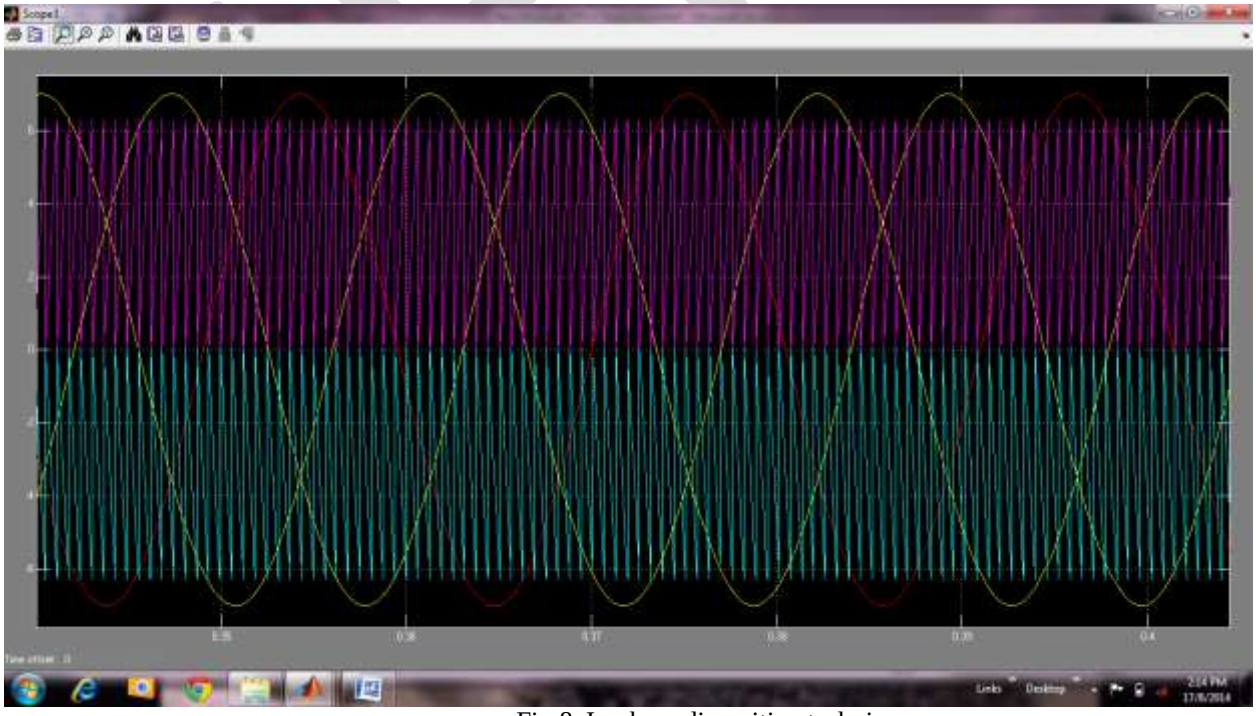


Fig.8. In-phase disposition technique

V/*f* CONTROL THEORY

Fig.7. shows the relation between the voltage and torque versus frequency. The voltage and frequency being increased up to the base speed. At base speed, the voltage and frequency reach the rated values. We can drive the motor beyond base speed by increasing the frequency further. But the voltage applied cannot be increased beyond the rated voltage. Therefore, only the frequency can be increased, which results in the field weakening and the torque available being reduced. Above base speed, the factors governing torque become complex, since friction and wind age losses increase significantly at higher speeds. Hence, the torque curve becomes nonlinear with respect to speed or frequency.

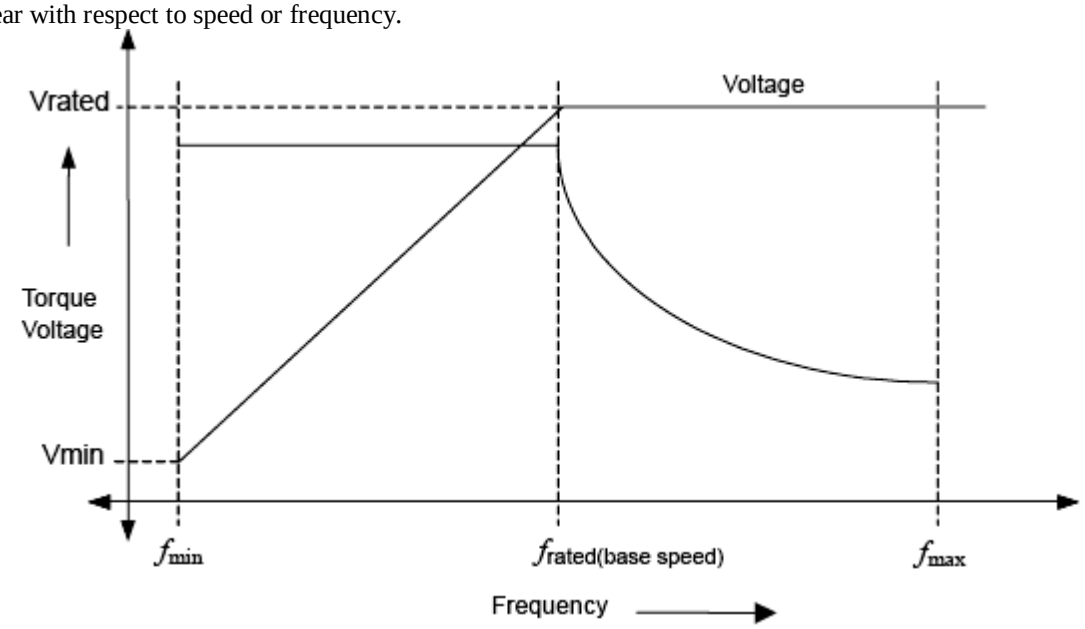


Fig.9. Speed-Torque characteristics with V/*f* control.

SIMULATED CIRCUITS AND WAVEFORMS

Fig.8. shows the PWM circuit to generate the gating signals for the multilevel inverter switches. To control a three phase multilevel inverter with an output voltage of three levels; two carriers are generated and compared at each time to a set of three sinusoidal reference waveforms. One carrier wave above the zero reference and one carrier wave below the reference. These carriers are same in frequency, amplitude and phases; but they are just different in dc offset to occupy contiguous bands. Phase disposition technique has less harmonic distortion on line voltages.

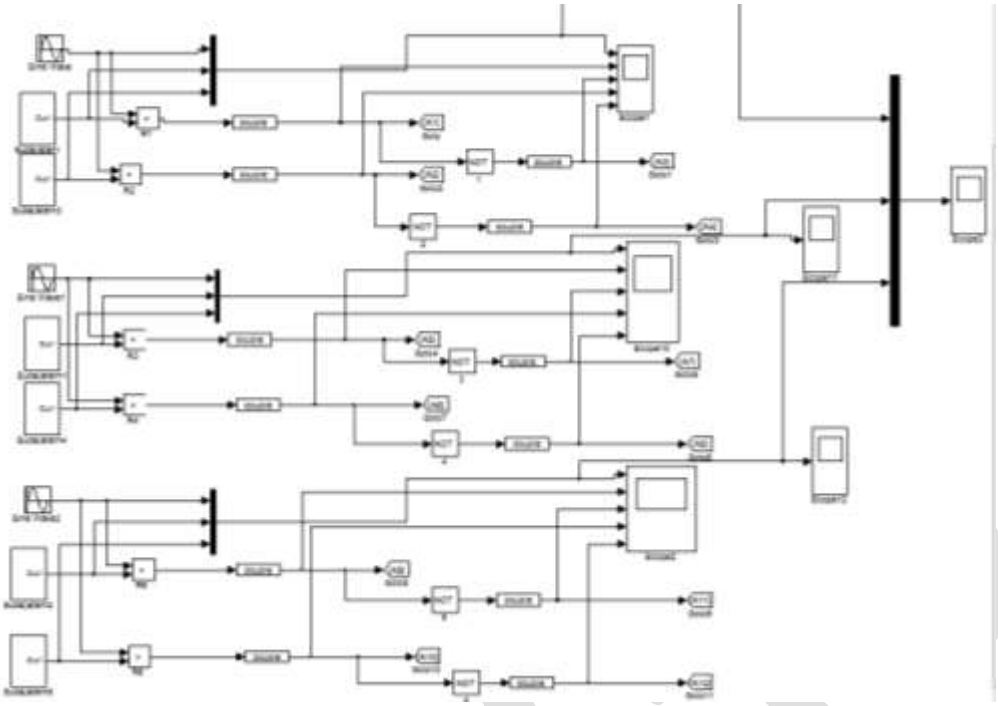


Fig.10. PWM simulation circuit.

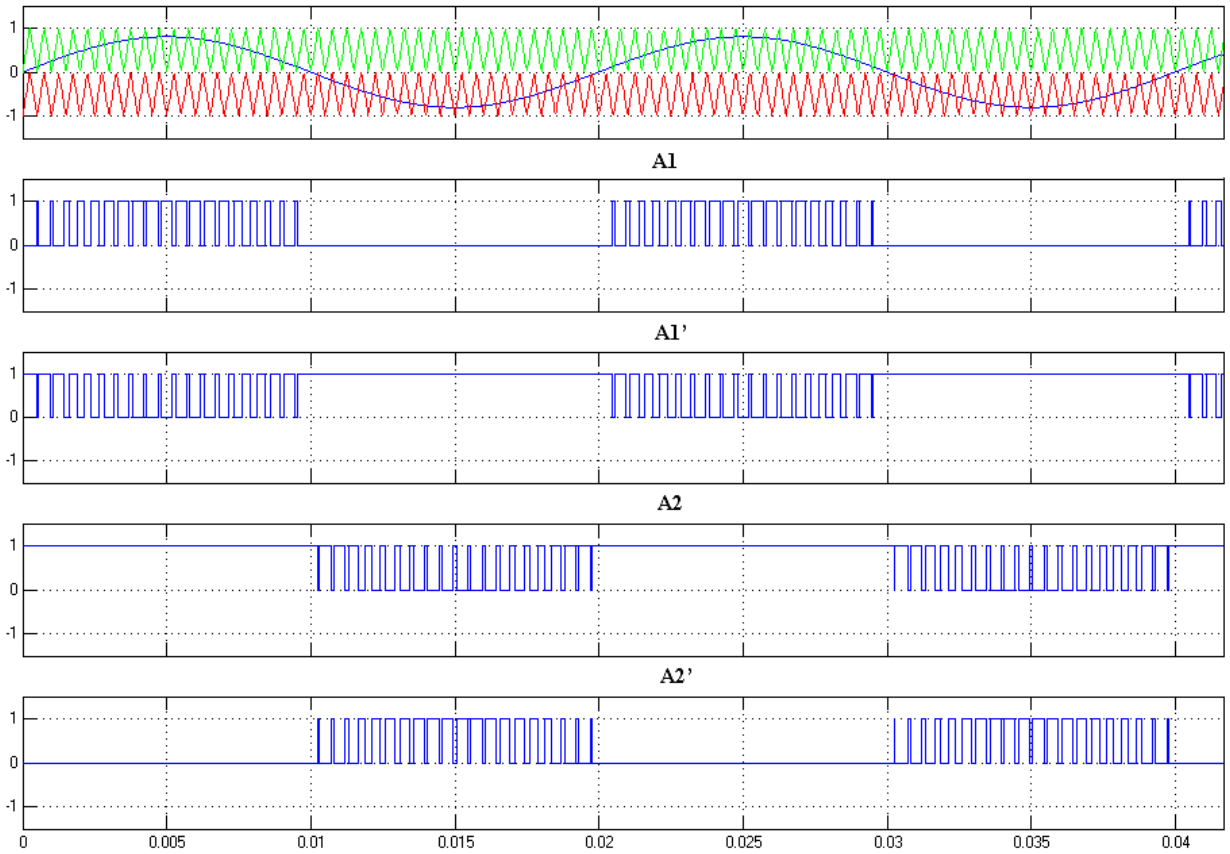


Fig.11. Gate pulses for leg A switches.

Fig.11. shows the waveform of sine-triangle intersection. Two carriers together with modulation signal have been used to obtain SPWM control. Simulated model for entire circuit is shown in Fig.12.

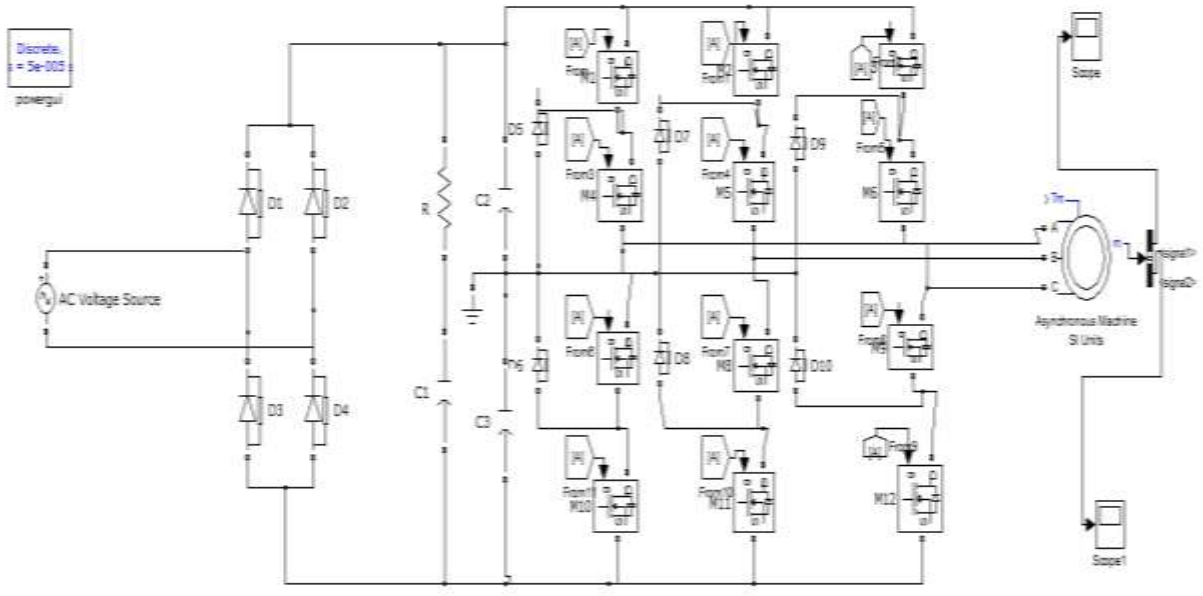


Fig.12. Simulated circuit.

Output voltage and current waveforms for 50 Hz frequency are shown in below figures 13 and 14.

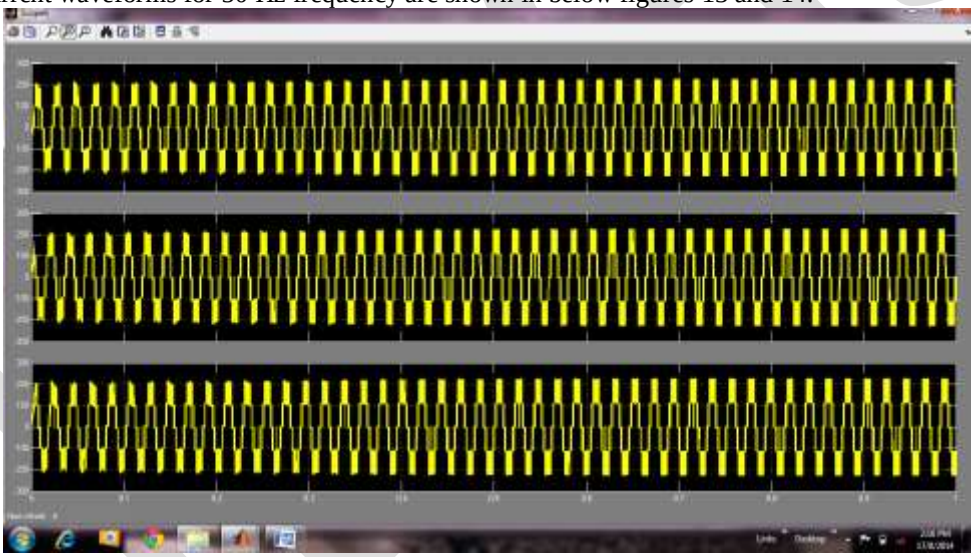


Fig.13. Output line-line voltage for 50Hz frequency.

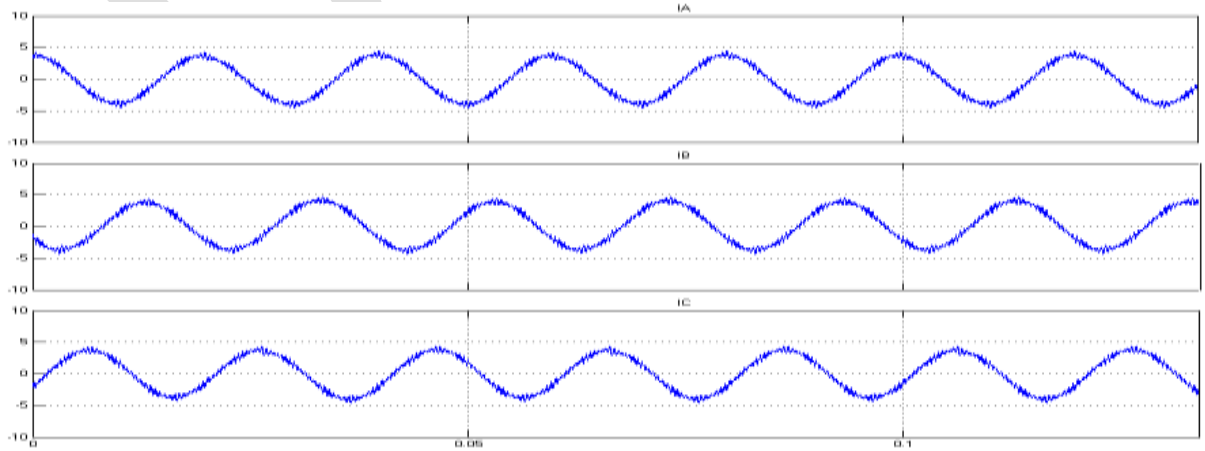


Fig.14. Output current waveform.

The FFT plot of the output voltage is shown in Fig.15. The plot shows that the harmonic content present in the output voltage is very low.

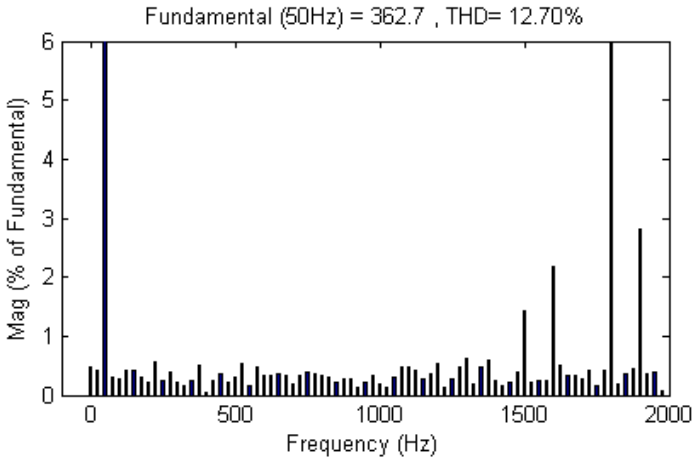


Fig.15. FFT for output voltage.

Speed-Torque curves for 50 Hz and 45 Hz frequencies are shown in figures 16 and 18.

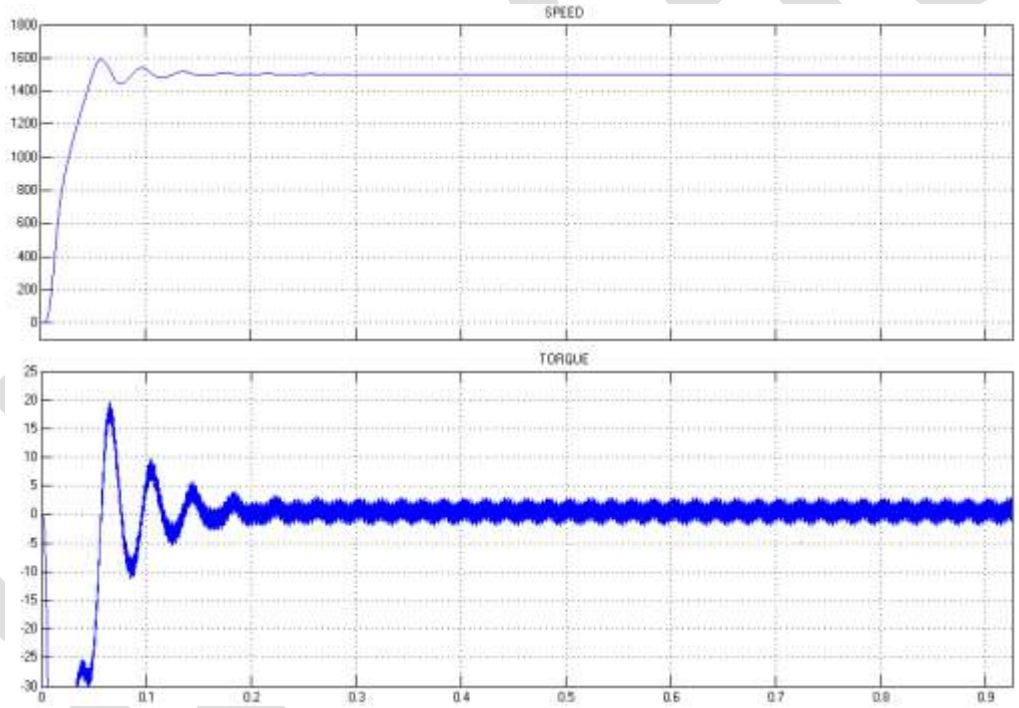


Fig.16. N-T curves for 50Hz frequency.

The frequency of reference signal determines the inverter output frequency; and its peak amplitude controls the modulation index. The variation in modulation index changes the rms output voltage of the multilevel inverter. By varying the reference signal frequency as well as modulation index, the speed of an induction motor gets controlled.

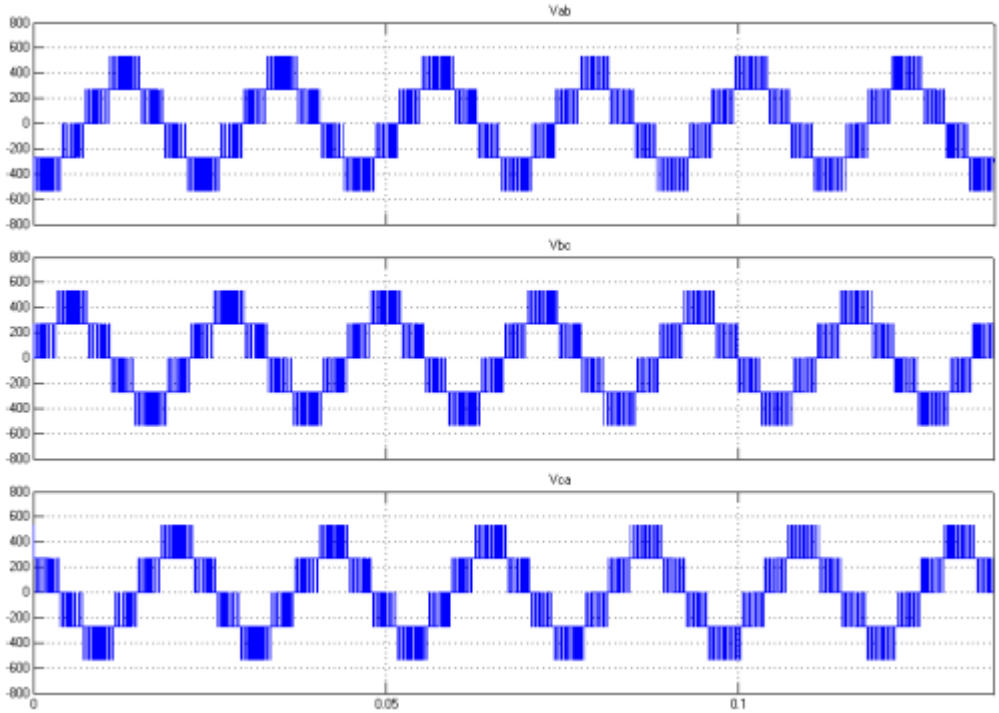
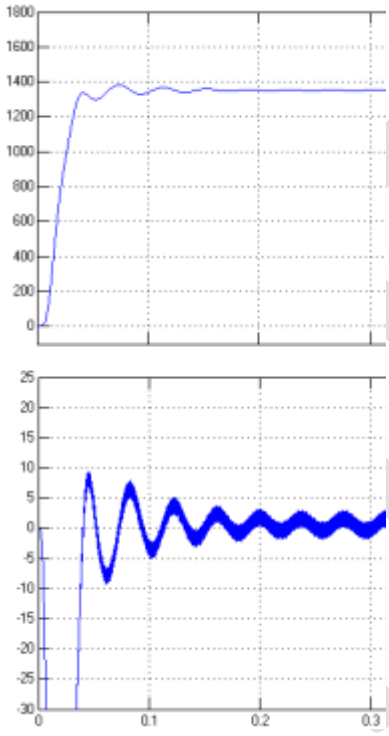


Fig.17. Output line-line voltage for 45Hz frequency.



		THD(%)	
Frequency (Hz)	Speed (rpm)	Current (Ia)	Voltage (Vab)

Fig.18. N-T curves for 45Hz frequency.

The speed-torque curves conclude that the voltage and frequency applied to the motor gets decreased; then the speed of an induction motor also decreased simultaneously.

50	1479	3.33%	11.43%
45	1300	3.09%	10.97%
40	1275	7.89%	18.20%
35	1065	10.76%	27.30%

TABLE 2 Speed range for different frequency values.

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CONCLUSION

In this paper a diode clamped multilevel inverter has been presented for drive applications. The multicarrier PWM technique can be implemented for producing low harmonic contents in the output, hence the high quality output voltage was obtained. The open loop speed control was achieved by maintaining V/*f* ratio at constant value. The simulation results show that the proposed system effectively controls the motor speed and enhances the drive performance through reduction in total harmonic distortion (THD). This drive system can be used for variable speed applications like conveyors, rolling mills, printing machines etc.

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