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Harmonics Elimination PWM (HEPWM)

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ABSTRACT –--This paper proposes PWM Multi Level inverter to take advantage of the cascaded H-bridges inverter by utilizing all of the levels in the inverter even at low modulation indices. In order to deal with harmonic elimination, a sine wave is compared with carrier triangular wave is presented. This approach requires a modified carrier waveform that can be calculated based on short functions requiring only depth of modulation. The results show the viability of obtaining practically sinusoidal output waveforms, which are highly desirable in most inverter applications. The improvements in harmonic spectrum are pointed out, which prove the validity of the multilevel modulation.

Key Word –PWM inverter, Multi level inverter, harmonics elimination, sinusoidal pulse width modulation, THD, motor drives, and active power filters.

INTRODUCTION

Pulse width modulation is a method that is widely used now as a switching pulse to turn on and off the thyristors to give alternating current waveform at the output of an inverter circuit. The output waveform of an inverter will be a square-wave and contains harmonics from the 3rd harmonics, and as the 3rd harmonic located very close to the fundamental frequency and very difficult to filter it as we need to design very high order filter, therefore nowadays we prefer to use PWM method to reduce the total distortion because of the harmonics or simply called THD. To generate the PWM signal, we need two signals and compare both, a modulating sine-wave signal with let say 50Hz frequency and the carrier triangular-wave signal with frequency higher than the modulating signal frequency. With PWM method, the 3rd harmonic will appear not at the 3 times frequency of the fundamental but actually at the frequency of the carrier signal, therefore in designing the PWM, we need to use higher frequency for the carrier signal but lower frequency for the modulating signal.

Multilevel inverters have been proposed for such uses as static var compensation, motor drives, and active power filters. For many of these applications, multilevel inverters will operate in the low amplitude modulation index region, and some levels of the inverter will go unused most of the time if conventional multilevel carrier-based PWM techniques are used [1].

There are three topologies of multilevel inverters-cascaded, flying capacitor and diode clamped, each having its own advantages in various applications. Cascaded H-Bridge multilevel inverter is one of the popular converter topologies used in high-power-medium-voltage (MV) drives. The cascaded inverter type dynamic voltage restorer with neural control strategy is proposed [2]. The H Bridge cells are normally connected in cascade on their ac side to achieve medium-voltage operation and low harmonics distortion

The industry requires power equipment increasingly high, in the megawatt range. The rapid evolution of semiconductor devices manufacturing technologies and the designer's orientation has enabled the development of new structures of converters (inverters) with a great performance compared to conventional structures. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverters. a multilevel converter not only achieves as high power ratings. But also enables the use of renewable energy sources [3]. Recent advances in power electronics have made the multilevel concept practical [4]. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. Furthermore, several IEEE conferences now hold entire sessions on multilevel power conversion. It is evident that the multilevel concept will be a prominent choice for power electronic

systems in future years, especially for medium-voltage operation. Finally, the simulation of a multilevel PWM single phase inverter is designed and harmonics elimination analysis is achieved.

MULTI LEVEL INVERTER STRUCTURES

As previously mentioned, three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. it should be noted that the term multilevel converter is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode. The multilevel inverter structures are the focus of in this paper. A seven level single phase cascaded inverter consists of three full bridges connected in series on the AC side. Each bridge can create three different voltage levels. Due to switch combination redundancies, there are certain degrees of freedom of how to generate the multilevel AC output voltage. The AC outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels L in a cascade inverter is defined by **L= 2s+1**, where **s** is the number of separate DC sources.

Each H-bridge is fed with the same value of DC voltage hence it can be called as symmetrical cascaded multilevel inverter. Each full bridge inverter can generate three different voltage outputs: +Vdc, 0, and –Vdc. The phase output voltage is synthesized by sum of three inverter outputs, van= va1+ va2+ va3. (1)

The seven-level output waveform is obtained by different switching combinations. For a stepped waveform such as the one depicted in **Figure (1b)** with s steps, the Fourier Transform for this waveform follows [5, 6]:

$$V(wt) = \frac{4\text{Vdc}}{\pi} + \sum_{n=1,3,5\ldots} (\cos(n\theta 1) + \cos(n\theta 2) + \cos(n\theta 3) + .. + \cos(n\theta s)) \frac{\sin(nwt)}{n}, \quad n=1, 3,5,7,9 \ldots \quad (2)$$

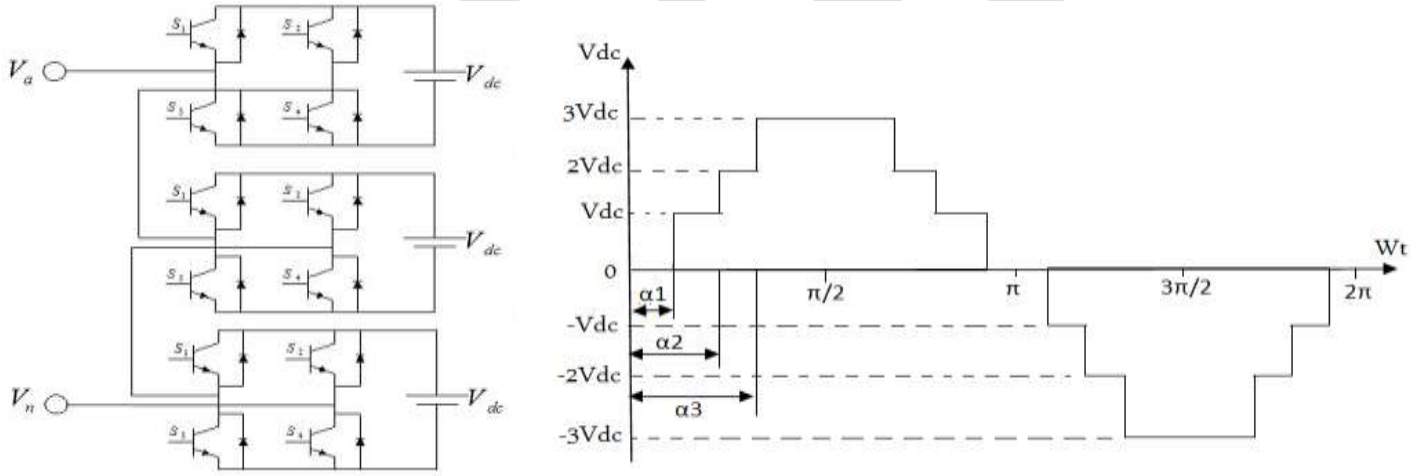

FIGURE 1.a) SINGLE-PHASE STRUCTURE OF A SEVEN CASCADED H-BRIDGES INVERTER, b) OUTPUT PHASE VOLTAGE WAVEFORM OF 7-LEVEL CASCADE INVERTER WITH 3 SEPARATE DC SOURCES

From eq. (2), the magnitudes of the Fourier coefficients when normalized with respect to Vdc are as follows:

$$H(n) = \frac{4c}{n\pi} + [\cos(n\theta 1) + \cos(n\theta 2) + \cdots + \cos(n\theta s)], \quad , n=1,3,5,7,9,... \quad (3)$$

The conducting angles, θ1, θ2,..., θs, can be chosen such that the voltage total harmonic distortions a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated [7].

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows [8, 9].

Advantages:

- The number of possible output voltage levels is more than twice the number of dc sources (L= 2s+ 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

- Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple DCSs readily available.

The cascaded inverter as shown in Figure (1a) has 12 inverter states which allow bi-directional current flow and a fixed inverter output voltage. They are listed in Table (1).

SWITCHING STATE	VOLTAGE Van						
	+V	+2V	+3V	0	-V	-2V	-3V
S1	1	1	1	0	0	0	0
S2	1	1	1	1	0	0	0
S3	0	0	0	0	1	1	1
S4	0	0	0	1	1	1	1
S5	0	1	1	0	0	0	0
S6	1	1	1	1	1	0	0
S7	0	0	0	0	0	1	1
S8	1	0	0	1	1	1	1
S9	0	0	1	0	0	0	0
S10	1	1	1	1	1	1	0
S11	0	0	0	0	0	0	1
S12	1	1	0	1	1	1	1

TABLE 1 INVERTER STATE OF CASCADED SEVEN LEVEL INVERTER

PULSE-WIDTH MODULATION PWM AND SIGNAL DEFINITIONS

The Pulse-width Modulated (PWM) inverter is the most favoured one for industrial applications. The control schemes of PWM inverters are broadly classified as programmed PWM inverters and sinusoidal PWM inverters. The sinusoidal PWM method is very popular in many applications. Linear algebraic equations are solved to obtain the switching angles resulting in eliminating the unwanted harmonics.

Pulse-width modulation can take different forms. The pulse frequency is one of the most important parameters when defining a PWM method and can be either constant or variable. A constant-frequency (CF) PWM signal can be produced simply by comparing a reference signal, r (t), with a carrier signal, c (t), as depicted in Figure(2).

Three types of carrier signals are commonly used in constant-frequency PWM:

1. Sawtooth Carrier, reported in Figure(2.a): The leading (rising) edge of PWM output occurs at fixed instants in time while the position of the trailing (falling) edge is modulated as the reference signal level varies. Hence the method is also called constant-frequency trailing-edge modulation.

2. Inverted Sawtooth Carrier, reported in Figure(2.b): The trailing (falling) edge of PWM output occurs at fixed instants in time while the position of the leading (rising) edge is modulated as the reference signal level varies. The method is usually referred to as constant-frequency leading-edge modulation.

3. Triangle Carrier, reported in Figure (2.c): Both the leading edge and the trailing edge of the PWM output is modulated. The rising and falling edge of the triangle are usually symmetric so that the pulse is centred within a carrier cycle when the reference is a constant. The method is called constant-frequency double-edge modulation.

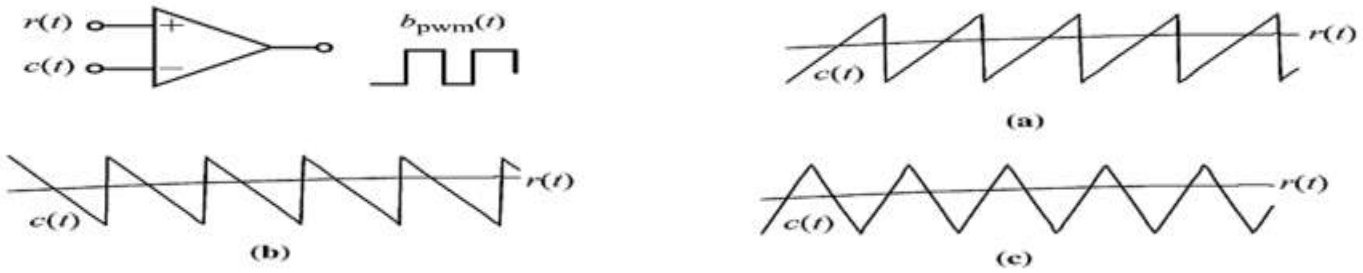

Figure (2) PULSE-WIDTH MODULATION, a) SAWTOOTH CARRIER ,b) INVERTED SAWTOOTH CARRIER, c) TRIANGLE CARRIER.

For AC–DC and DC–AC converters, the reference signal typically contains at least one sinusoidal component at the fundamental frequency of the AC input or output of the converter. For poly-phase converters, each phase will have a separate reference and their sinusoidal components are shifted from each other by the same phase angle that separates the input or output phase voltages. Often, the PWM references also contain harmonics of the fundamental component.

DESIGN CALCULATIONS AND CONSIDERATIONS

In order to eliminate 7 non-zero harmonics, we will need to obtain the angles from the earlier equation. And using the equations, we have 7 non-linear equations with 7 variables; now we need to use **eq. (1)** to calculate the angles using Newton- Raphson method of iteration. And finally we obtain the angles.

In general Fourier series is given by,

$$V(wt) = ao + \sum_{n=1}^{\infty}(ancosnwt + bnsin\,nwt) \quad (4)$$

In this case Fourier series expansion of output voltage waveform is given by

$$V(wt) = \sum_{n=1}^{\infty}(bnsin\,nwt) \quad (5)$$

Where a_o=a_n= 0 (due to quarter wave symmetry)

$$bn = \frac{1}{\pi}\sum_{0}^{2\pi} Vdc\ sin\ nwt\ dwt \quad (6)$$

$$bn = \frac{4Vdc}{n\pi}\cos n\,\alpha \quad (7)$$

$$bn = \frac{4Vd}{n\pi}\sum_{i=0}^{s} cos\ n\alpha\ i \quad (8)$$

Where the modulation index **M** is defined as

$$M = \frac{\wedge V1}{4Vdc} \quad (9)$$

For a 7-level inverter, the equations should be solved, and the switching angles must be less than π/2.

The Pspice schematic diagram of 7level inverter and comparator circuits is shown in Fig. (3) and Fig. (4), respectively.

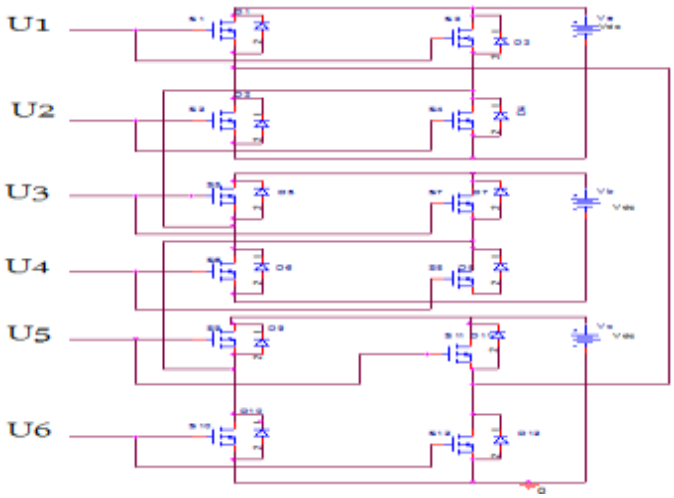

Figure (3) SINGLE PHASE SEVEN-LEVEL CASCADED MULTILEVEL INVERTER

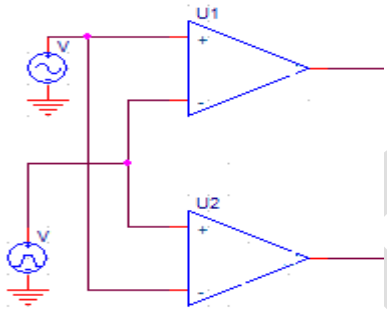

FIGURE (4) COMPARATOR

Figure (5) shows the input carrier and references waveforms and output comparator U1 and U2 waveforms.

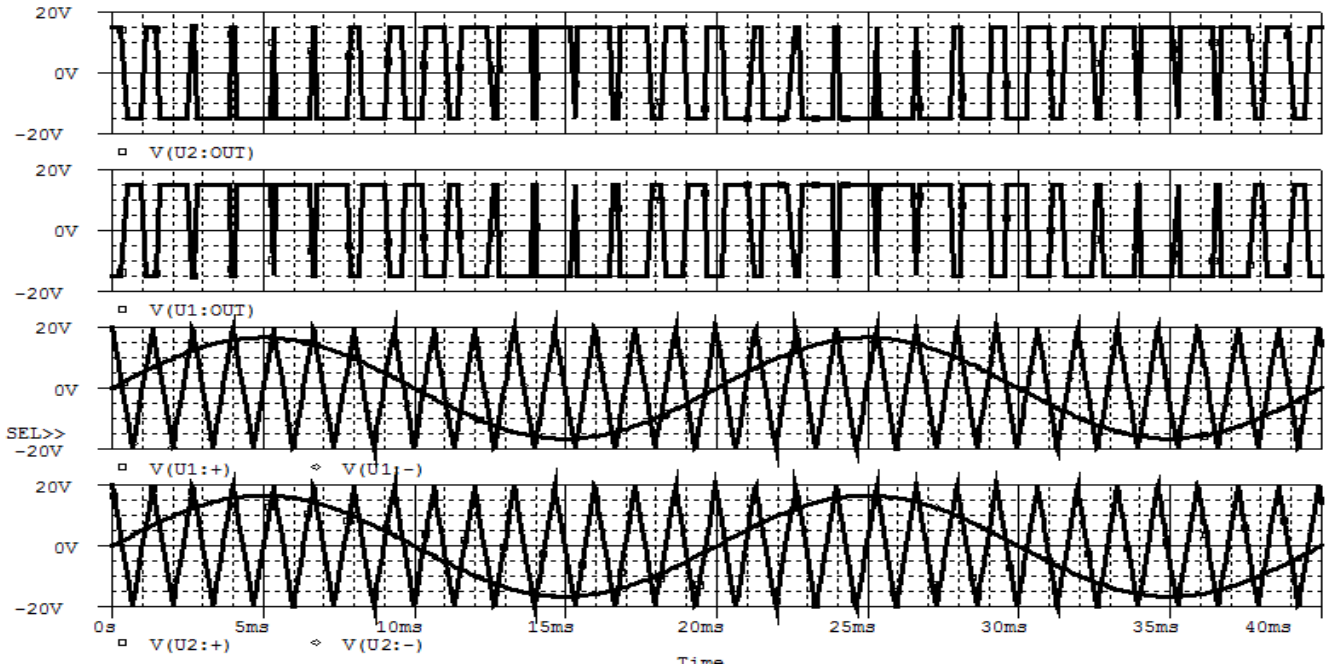

FIGURE (5) CARRIER AND REFERENCES WAVEFORMS AND OUTPUT COMPARATOR 1 AND 2 WAVEFORMS

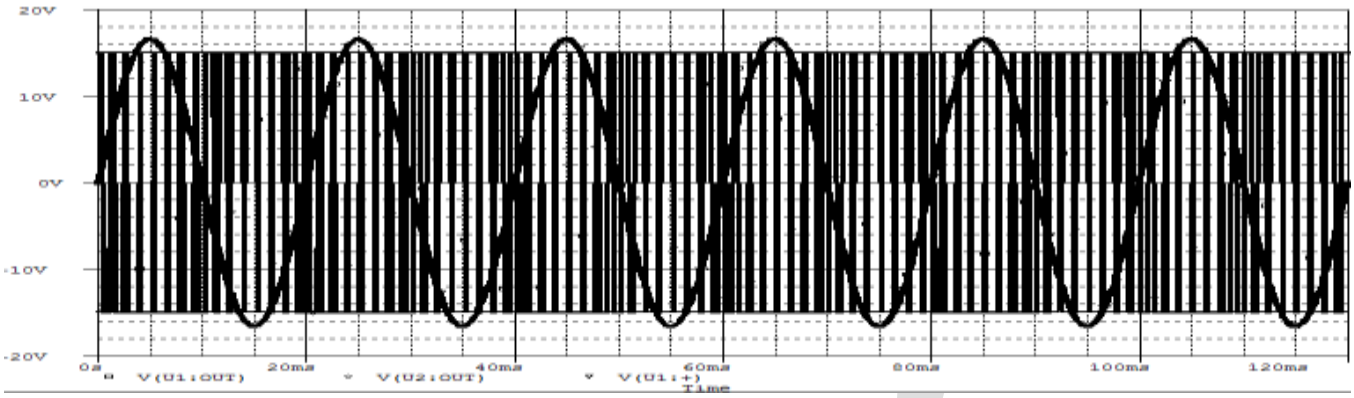

FIGURE (6) REFERENCES WAVEFORMS AND OUTPUT COMPARATOR U1 AND U2 WAVEFORMS.

SIMULATION RESULTS AND DISCUSSION

The simulation model of single phase seven level inverter is shown in Fig. (3). It consists of three full bridge inverters connected in series. The switching pulses are given from the switching circuit to the switches. The single phase AC output is given to the load. The input voltages for all the three full bridge inverters are same.

The THD values for different values of modulation index are shown in the Fig.7. From the Figure, it can be inferred that when modulation index is higher, the THD value is lower. Hence the simulation results are shown for M=0.8.

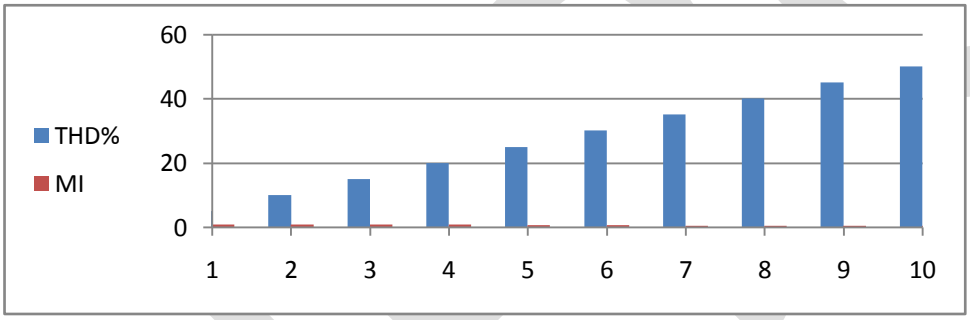

FIGURE.(7). THD FOR VARIOUS VALUES OF MODULATION INDEX

FIGURE (8) shows the Switching Pulses for Seven-Level Cascaded Multilevel Inverter Simulation with MI=0.83. and the input voltage was 100V for each bridge of multilevel inverter . The switching angles obtained using eq. (8), and given to the switching circuit whose output is given to switches of cascaded multilevel inverter.

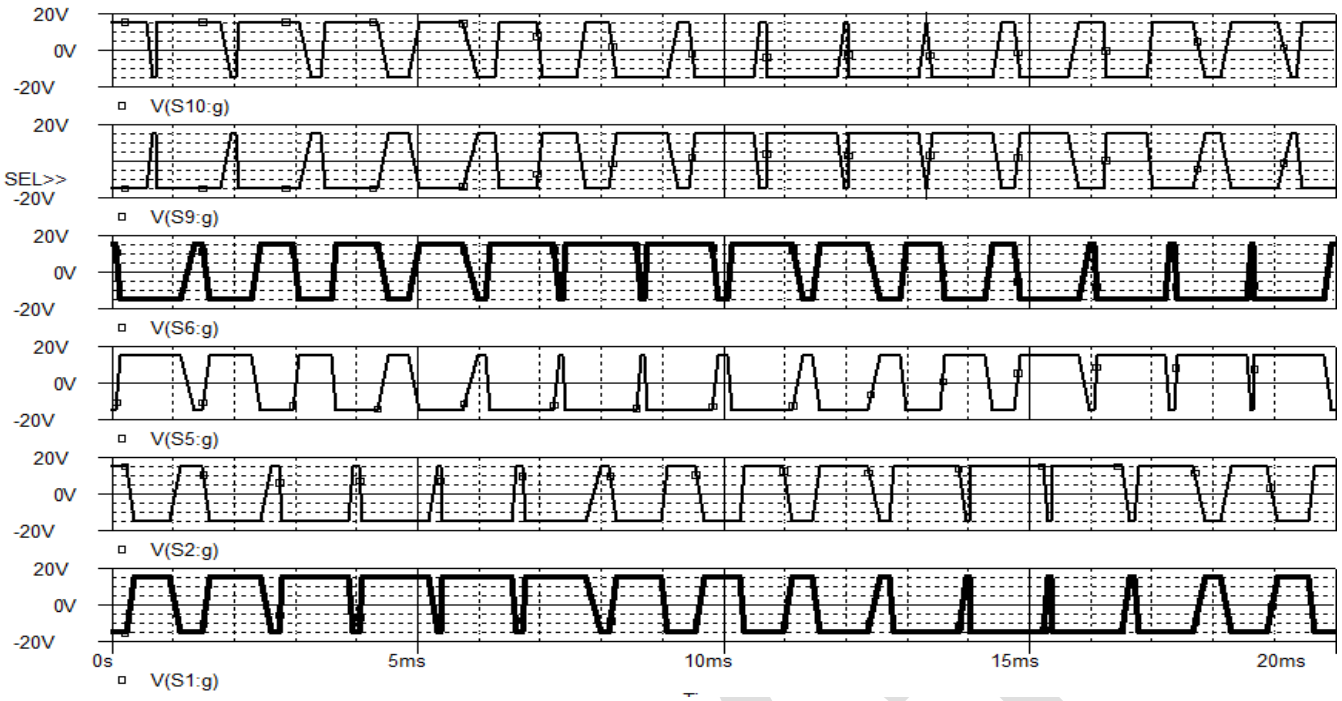

Figure (8): SWITCHING PULSES FOR SEVEN-LEVEL CASCADED MULTILEVEL INVERTER

The output voltage of the seven-level cascaded multilevel inverter is shown in Figure.(9).and Figure.(10).

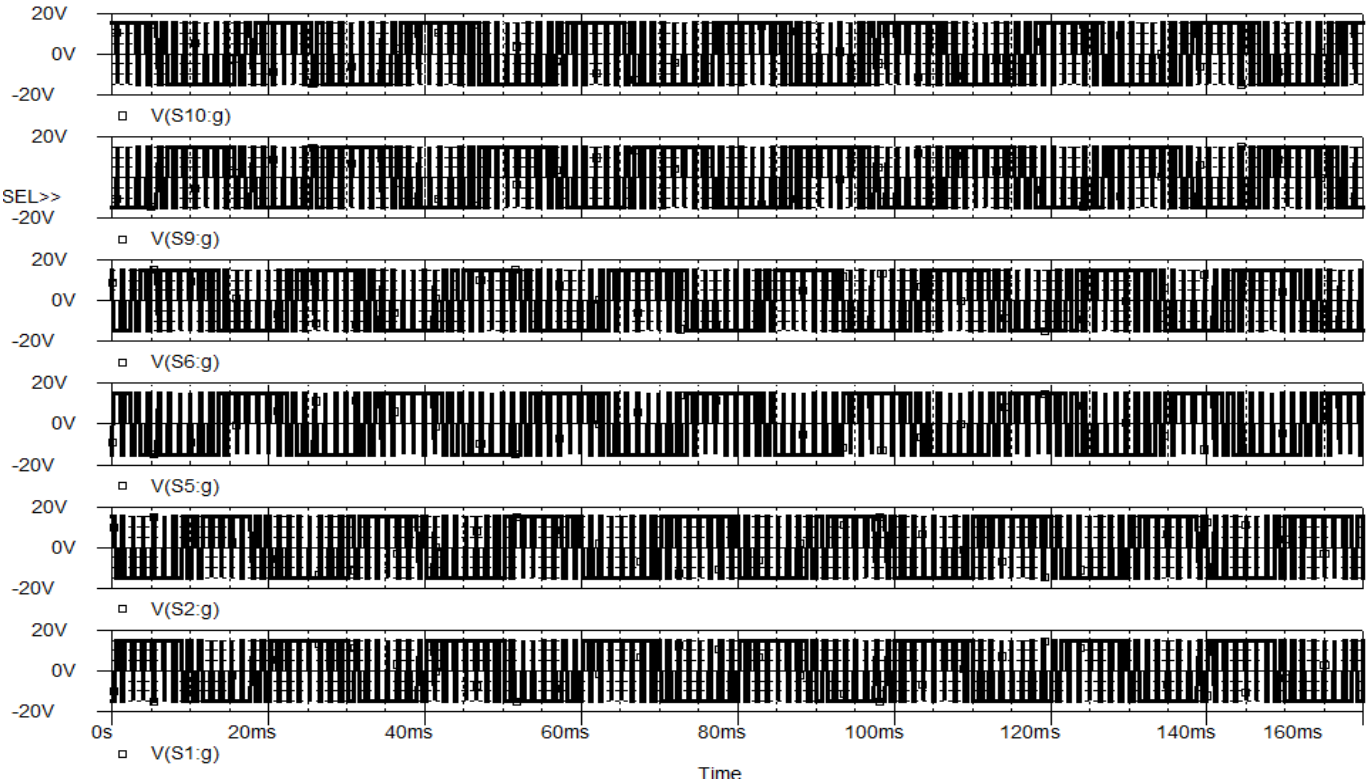

FIGURE (9) THE OUTPUT FOR EACH SWITCH

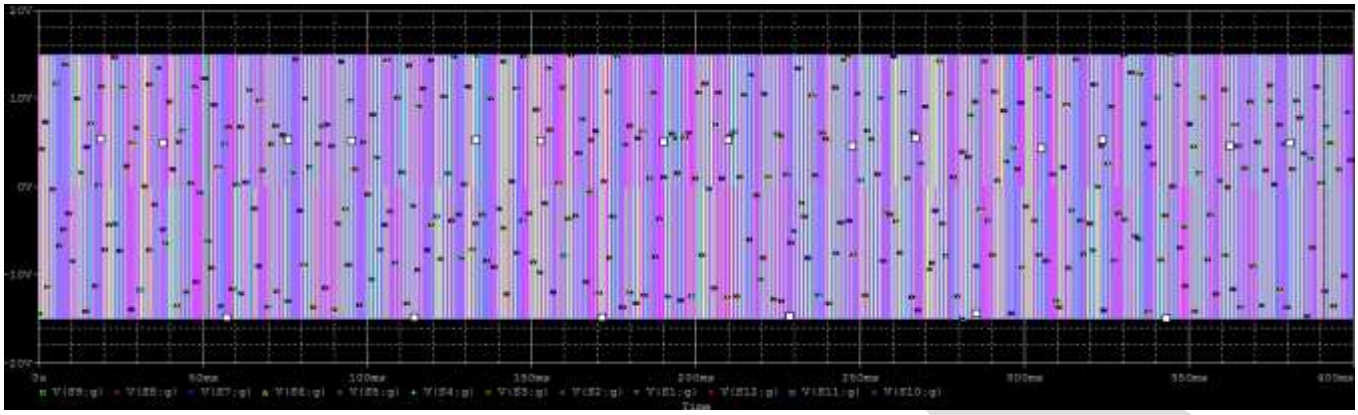

FIGURE (10) THE OUTPUT FOR ALL SWITCHES

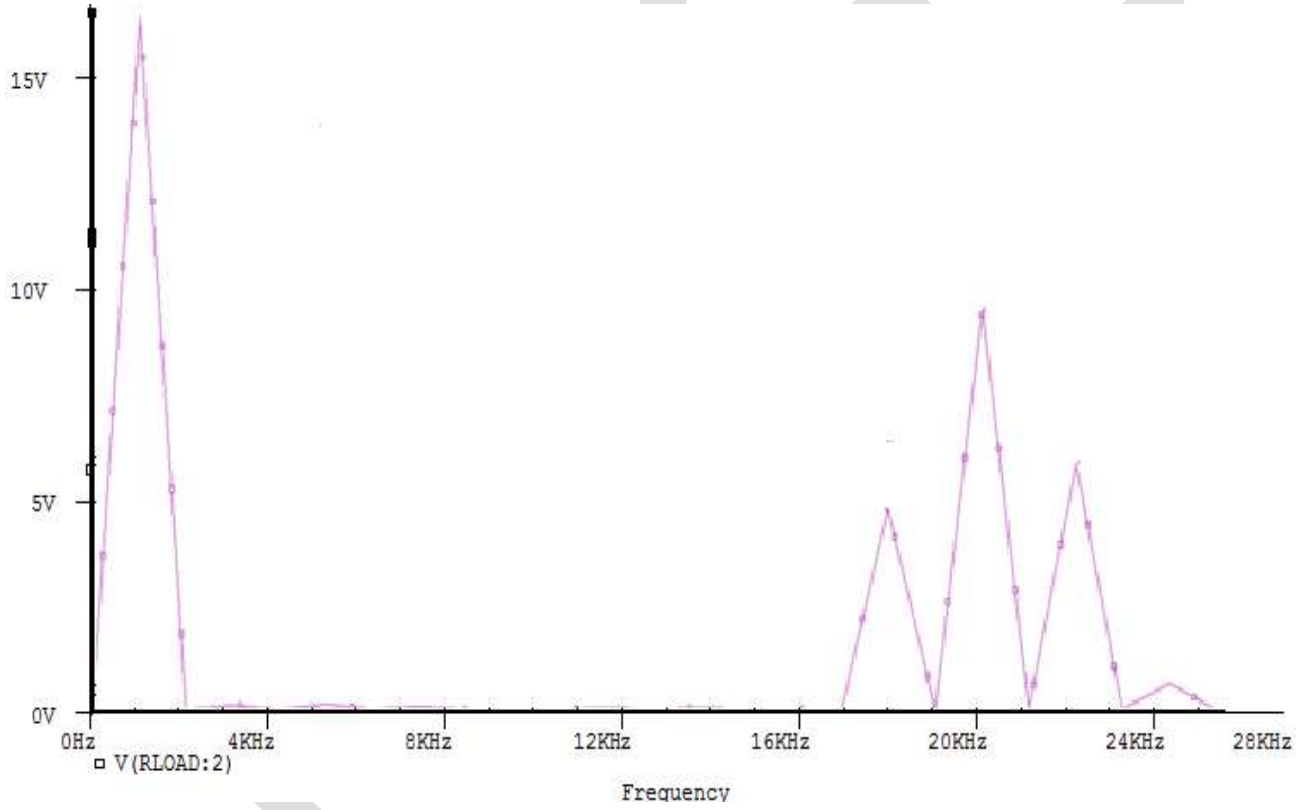

FIGURE 11: FREQUENCY SPECTRA OF THE CIRCUIT WITHOUT FILTER

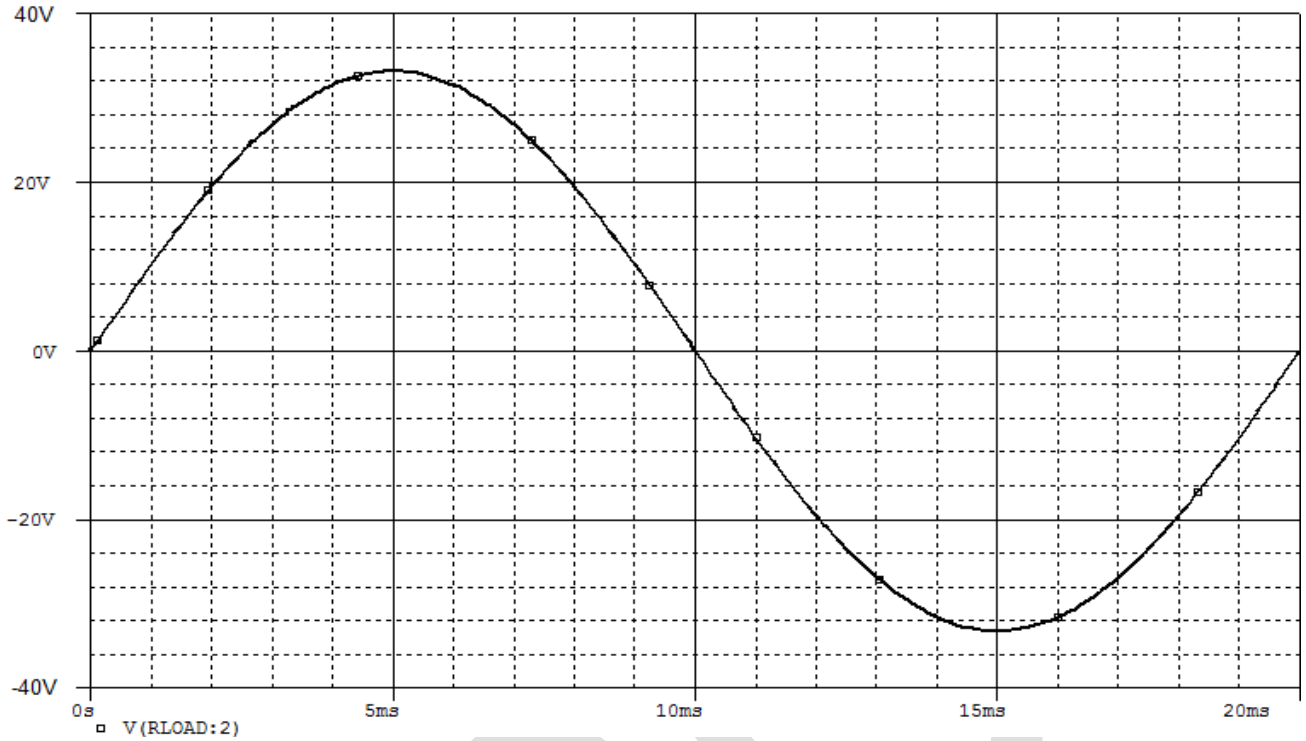

Figure (12)OUTPUT VOLTAGE ON THE LOAD WITH FILTER

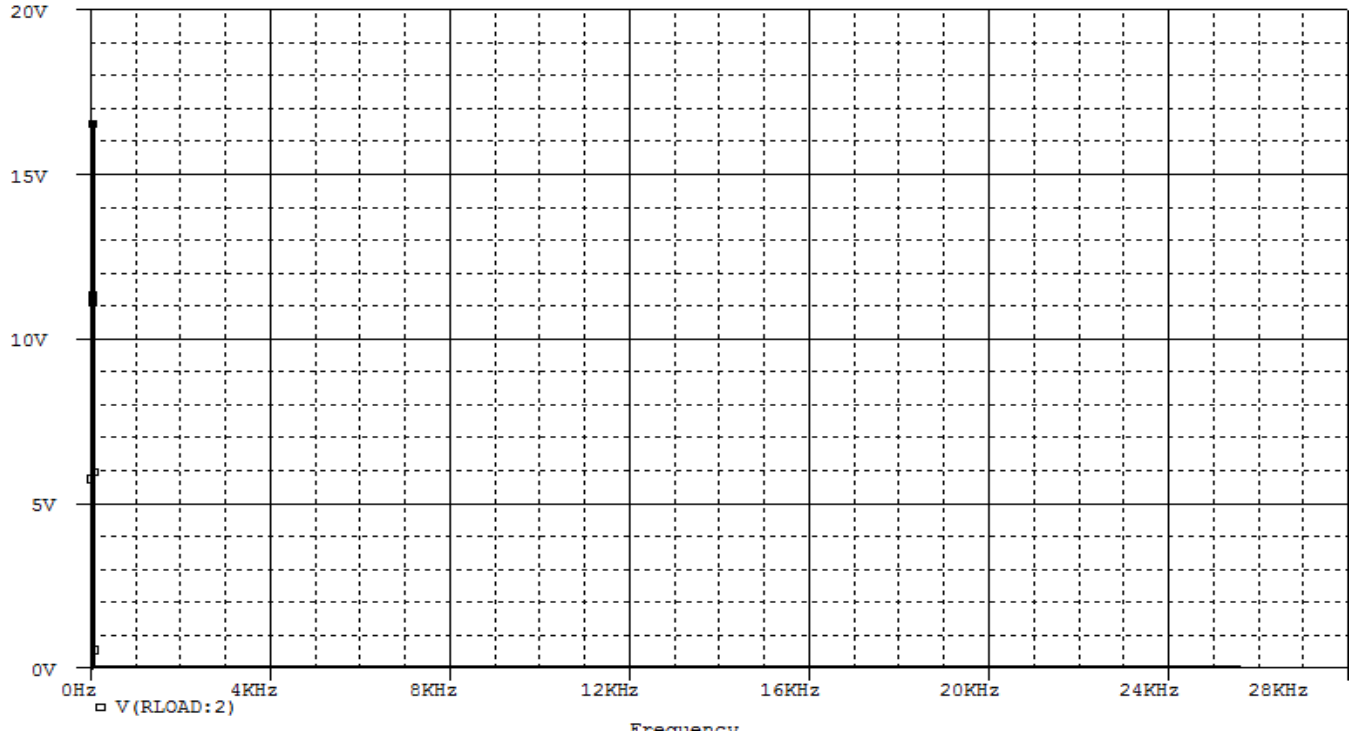

Fig (13) RLOAD FREQUENCY WITH FILTER.

CONCLUSION

In single inverter without filter is draw more harmonics, in this paper, the multilevel inverter designed by using Pspice software, and %THD was discussing. In this model PWM techniques along with LC filter were designed to bring down harmonics within its limit. As a result of study multilevel inverter single phase has greater advantage even without using filter design the harmonics are hidden to some level. Multilevel inverter can be used in high power application which has balanced voltage.

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