Fault Tolerant DC-DC Converter for DTG Servo Power Amplifier Supply

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ABSTRACT - Forward converter is one of the most studied topologies due to its lower ripple, lower parts count and hence high reliability. Owing to the need of miniaturization of Inertial Navigation System, a mini power module had to be developed for which forward converter topology was selected. A configuration of grouping the outputs into HMCS was attempted. The converter for DTG servo power amplifier had to supply the current demanded by the sensor electronics which is dynamic. Interleaved forward converter provides a better solution to satisfy the increased power and dynamic load conditions. As an added advantage, though one portion gets faulty, the other portion can provide half the maximum load, giving continuous power. The paper discusses the benefits of interleaving in the converter supplying the servo power amplifier experiencing dynamic load conditions and simulations for both single and interleaved converter design validation.

Keywords— Interleaving, Dynamic Load, Hybrid Micro Circuit (HMC), Stresses, Dynamically Tuned Gyroscopes (DTG), Flux imbalance, phase shifted control

INTRODUCTION

Inertial Navigation System (INS) consists of inertial sensors: Dynamically Tuned Gyroscopes (DTG) and Ceramic Servo Accelerometers (CSA) and its associated Electronics. As part of developing miniature Inertial Navigation System (mINS), a mini power module had to be developed. For the ease of miniaturization, forward topology was selected and it offers additional merits like low output voltage ripple and low input r.m.s current [1]. A configuration in which the outputs were grouped into 3 types of Hybrid Micro Circuits (HMCs) was proposed. The servo loop power amplifier of the sensors experiences dynamic loads which has to be met by the +30V/1.25A converter. Interleaving of converters is a good choice to meet the dynamic load conditions and also has an advantage that though one converter gets faulty the other converter takes up half the maximum load giving uninterrupted power. The interleaving of converters distributes the current stresses and power loss in each converter cell [3]. Interleaved PWM can balance the current rating on the switches in each converter cell. Interleaving [8] also distributes power losses and thermal stresses of semi conductors due to smaller power processed through independent power stages. Interleaving means to parallel the stages so that they share common filter capacitor [8].

The key benefits [2] of interleaving are:

1. Reduced r.m.s current in the input capacitors
2. Ripple current cancellation at the output capacitor
3. Reduction of peak currents in primary and secondary of transformer
4. Improved transient response
5. Reduced EMI due to reduction in peak currents.

The paper discusses the comparison of forward, interleaved and push pull topologies, design of interleaved as well as single converter in case of the +30V/1.25A converter and SABER simulations to validate the design.

COMPARISON

A. Single Forward Converter

A single forward converter consists of a single switch and derived from a buck converter, forward converter delivers power from input source to the load during the on time of the switch and it is one of the discussed topologies [4]. Also for miniaturization purposes, due to lower parts count accompanied by low output voltage ripple, forward converter is a designer's choice.

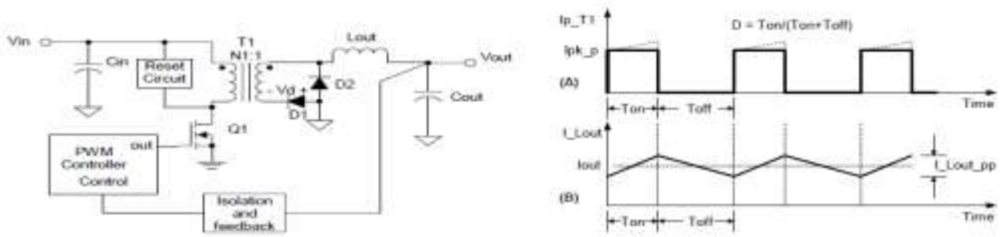


Fig. 1 Single Forward Converter

To reduce size and weight of magnetic components, frequency can be increased but at the cost of increased switching and core losses and EMI [1]. The single transformer and inductor are designed to carry the full peak current. In forward converters duty cycle and voltage stresses are restricted by each other [6], higher duty cycle means higher stresses on switches and lower stresses on the corresponding secondary diodes.

B. Interleaved Forward Converter

In interleaved forward converter the switches are driven by phase shifted control signals and current through switches is only a fraction of the input current[9]. Also input current ripple and conduction losses are reduced giving improved efficiency. Each converter carries only half of current and hence shares the total power.

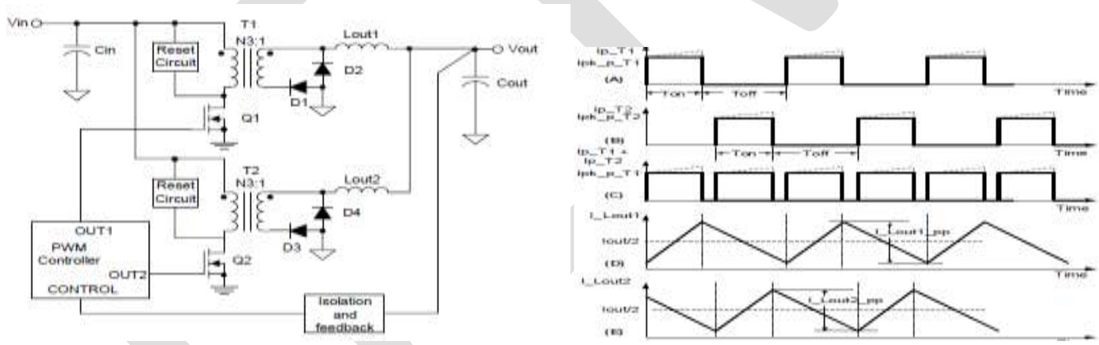


Fig.2 Interleaved Forward Converter

The two converter modules are operated through phase shifted PWM scheme so that output inductor current partially cancels each other. Therefore ripple voltage on output capacitor is reduced. By equal phase shift among paralleled stages, output filter capacitor ripple is lowered due to ripple cancellation effect. When the converters are paralleled, both of them share a common output capacitor and the distributed magnetic structure and minimum output filter size makes interleaving options attractive for high power density and low profile packaging. Multi converters can increase the equivalent duty cycle of the total module [6]. Also as intensity of EMI is proportional to peak currents, an interleaved converter of same total power as a single forward converter generates less EMI [5].In case one converter gets faulty, other converter takes up the service and support the nominal load though it cannot take up the occasional peak load. This is very important in case of the dynamic loads experienced by the DTG.

Two transformers are smaller than for a single forward converter but the two transformers occupy more volume and cost than a single transformer.

C. Push Pull Vs Interleaved Converter

A push pull converter consists of two forward converters connected in anti phase. When one transistor switches on, flux swings in one direction of B-H curve, in order to reverse direction the first transistor switches off and second transistor switches on. In order for the two areas of the flux density to be equal, the saturation and switching characteristics of the switching transistors must be identical under all working conditions and temperatures. A phenomenon common in push pull converters is flux walking [8]. If the transistor characteristics are not identical, "flux walking" to one direction of B-H curve occurs driving the core into the saturating region. If one of the two switches of the converter fails, the core does not get reset and continues to move along the same direction of BH curve. Saturation of the core leads to high collector current spike in one of the transistors. This excessive current produces large amounts of power loss in the transistor heating it up which further unbalances transistor characteristics, thus saturating core even more, producing saturation currents. This cycle continues until transistor goes to thermal runway, which leads to destruction.

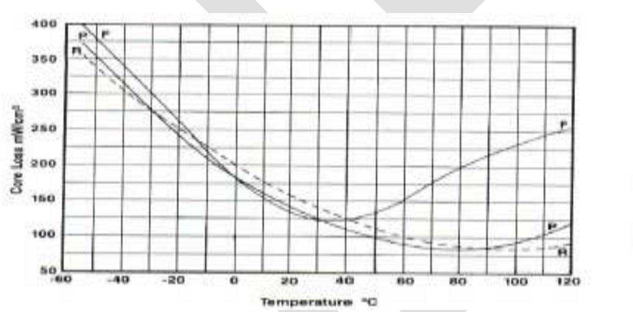
When compared to push pull, the certainty that there is no flux imbalance problem in interleaved forward converter is the best argument for its use. Also in case of an interleaved converter when one converter gets faulty, the current through the switch can be sensed and the faulty portion can be isolated whereas in push pull converter isolation is meaningless as flux imbalance cannot be overcome. The converters are connected in parallel and in case if one fails, the other would function as an independent converter supporting half the maximum load.

DESIGN

Design includes design of transformer (core and number of turns), output filter, switch and its controller for both single and interleaved configuration.

A. Core Selection

Ferrite R material is chosen as the core material due to operation at high frequencies and increased resistivity. The core curves[7] of the various materials are given below.



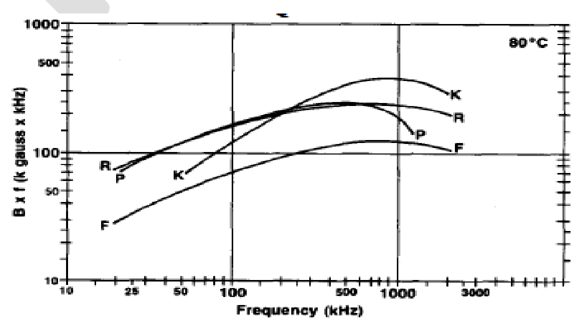


Fig.3. Curves for Various Cores

The parameters for the design are briefed below:

TABLE I: DESIGN SPECIFICATIONS

Parameters	**Single**	**Interleaved(Per Phase)**
V_{in}	28 V	28 V
V_{out}	30 V	30 V
I_{out}	1.25 A	0.625 A
P_{out}	37.5 W	18.25 W
I_{out}	1.25 A	0.625 A
F_{sw}	400 KHz	200 KHz

In a single forward converter the core selection is based on full output power whereas in case of interleaved core is chosen for half output power as each transformer supplies only half the output power.

$$\text{Transformer area product } A_p = \frac{\sqrt{D_{max}} \text{ x } P_{out} \text{ x } (1+1/n)}{K_w \text{ x } J \text{ x } 10^{-6} \text{ x } B_m \text{ x } F_{sw}} \quad (1)$$

Converter is designed for a maximum of 62% duty cycle, efficiency of 80% and B_m: 0.12 T, J=3A/mm^2, Winding factor K_w=0.3.

B. Number Of Turns

Number of turns in primary
$$Np = \frac{V_{in} \text{ x } D_{max}}{B_m \text{ x } A_c \text{ x } 10^{-6} \text{ x } F_{sw}} \quad (2)$$

Turns ratio
$$T_{ratio} = \frac{V_o + V_d \text{ x } D_{max},}{V_{in} \text{ x } D_{max}} \quad (3)$$

Number of turns in secondary
$$N_{30} = T_{ratio} \text{ X } N_p \quad (4)$$

Number of turns in reset winding
$$N_{reset} = \frac{1- D_{max}}{D_{max}} \text{ X } N_p \quad (5)$$

D. Output Filter

$$L = \frac{V_{out}(1-D_{min})}{2xK \text{ x } I_{out} \text{x } F_{sw}} \quad (6)$$

$$C = \frac{K \text{ x } I_{out}}{8 \text{ x } F_{sw} \text{ x } V_{ripple}} \quad (7)$$

$$\text{Where } D_{min} = \frac{Vin_{min} \text{ x } D_{max}}{V_{in\ max}} \quad (8)$$

$$K = \frac{I_{ripple}}{I_{out}} \qquad (9)$$

E. Switch And Controller

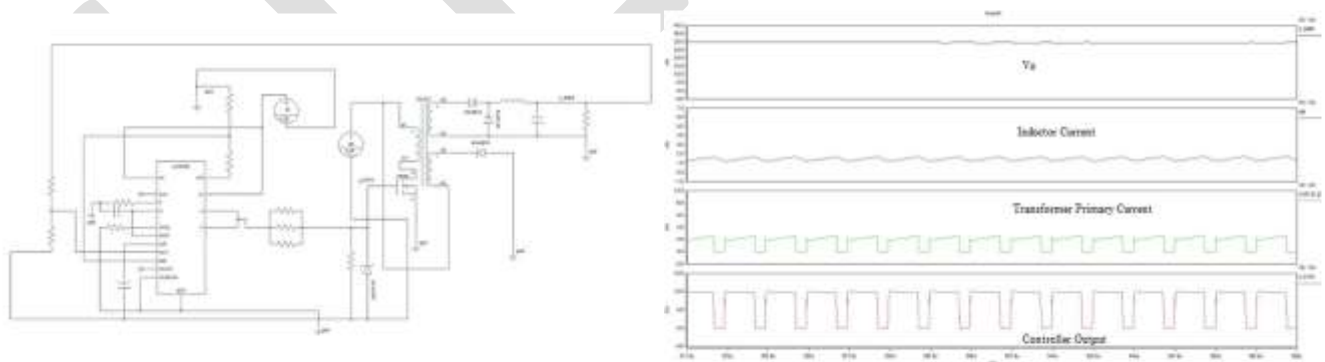
Due to lower on state resistance, MIL Grade IRFM3415 is selected as the switch and UC1525B is selected as the controller. The two outputs which are phase shifted from each other are used to feed the two switches of the interleaved converter. In single forward converter both these outputs are OR ed to obtain the required signal. So for a single converter the frequency is about 400 KHz and in interleaved converter each converter is designed for a frequency of 200 KHz.

TABLE II: OBTAINED VALUES

Values	**Single**	**Interleaved**
Core	42106 TC	42106 TC
N_p	15	31
N_{30}	27	56
N_{reset}	9	19
L	39.3 uH	157 Uh
C	4 uF	4 uF

SIMULATION RESULTS

Simulations for both the configurations are done using SABER software and results were plotted. The controller output, transformer primary currents, inductor currents and output voltages have been observed.



(a)

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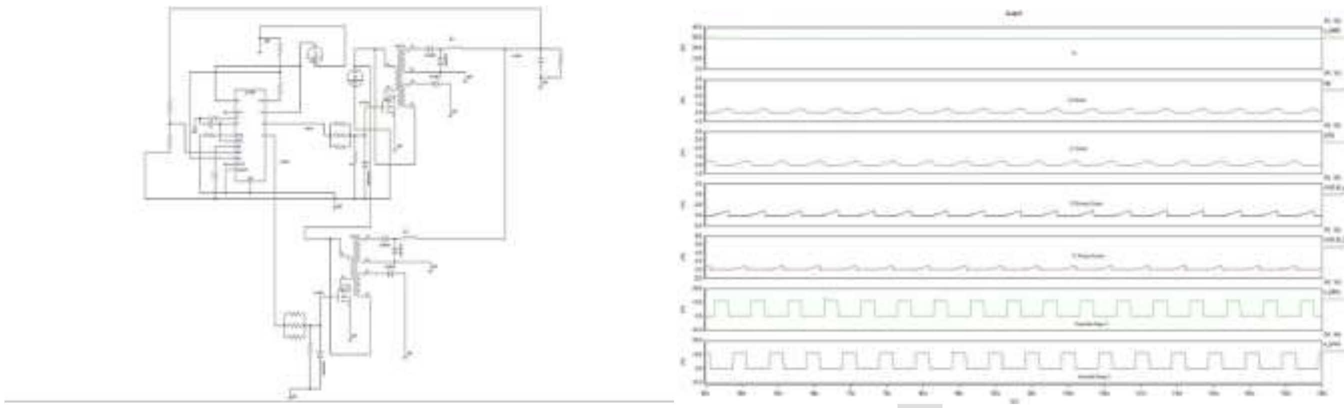

(b)

Fig.4 Simulation Results a) Single Forward Converter b) Interleaved Converter

It can be seen that the transformer primary and inductor currents are higher for single converter than the interleaved configuration. This highlights the benefits of interleaved converter over the single converter.

CONCLUSION

Both single and interleaved forward converter configurations were studied. Interleaving can be proposed as a fault tolerance measure to support the dynamic load conditions experienced by the system. The interleaving and single converter configurations were designed and validated through SABER software.

REFERENCES:

[1] C-M. Wang,C-M Lu,C-R. Lin,C-Yeh Ho, "A ZCS PWM Interleaved Forward Converter", *published in Future Energy Electronics Conference*,2013, pp. 344-348

[2] B.Shaffer, "Interleaving Contributes Unique Benefits to Forward and Flyback Converters" *in Proc. Unitrode Power Supply Des. Semin.New York*, 2005,pp. 5.1-5.30

[3] B.R Lin, W.C Li , K.L Shih, "Analysis and Implementation Of A Zero Voltage Switching Bi-Forward Converter", published in *IET Power Electronics*, 2009, Vol. 2, No.1,pp.22-32

[4] M. Brown, "*Power Supply Cookbook*", 2nd ed. USA Academic press, pp. 40-46, 2001

[5] Abraham.I.Pressman, "*Switching Power Supply Design*", pp.41-45,pp.89-92, McGraw-Hill publishers ,New York,199

[6] J.Zhang, H. Wu, Y.Xing, Y.Xia, K.Sun, "An Interleaved Series/Parallel Forward Converter With Wide Input Voltage Range", *published in Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 227-231

[7] Magnetics, "Magnetic Cores for Switching Power Supplies", pp 3-6, 2001

[8] T. Michael, M.Milan, C.Y. Fred, "Analysis and Evaluation of Interleaving Techniques in Forward Converters", *IEEE Transactions in Power Electronics*, 1998, Vol.13, No.4 , pp. 690-698

[9] B.R Lin, H.K Chiang, J.J.Chen, J-J, C.Y.Cheng, "Implementation of an Interleaved ZVS Forward Converter", *published in PEDS*, 2009, pp.854-859