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Design of Robust and Power Efficient Full Adder Using Energy Efficient Feed through Logic

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ABSTRACT – An Energy Efficient Feedthrough Logic (EE-FTL) is proposed in this paper to reduce the power consumption for low power applications. The EE-FTL is well suited to arithmetic circuits where the critical path is made of a large cascade of inverting gates. It has a unique characteristic where the output is pre-evaluated before the inputs from the preceding stage are ready. The proposed logic style requires low power when compare to the existing feedthrough logic (FTL). The proposed circuit is simulated and a comparison analysis has been carried out using 90-nm, 1.2V CMOS process technology. A CMOS Full Adder is designed by the energy efficient feedthrough logic and the simulation result in MicroWind environment shows that the proposed logic reduces the power consumption by 77%, 70% and 36% over FTL, Low Power FTL (LP-FTL) and Constant Delay Logic (CDL), respectively. The problem of requirement of inverter as in dynamic logic is completely eliminated in the proposed logic.

Keywords— Feedthrough logic(FTL), critical path, pre-evaluated, constant delay.

INTRODUCTION

Energy efficiency is one of the most required features for modern electronic systems designed for high-performance and portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. The invention of the dynamic logic in the 80s is one of the answers to this request as it allows designers to implement high performance circuit block, i.e., arithmetic logic unit (ALU), at an operating frequency that traditional static and pass transistor CMOS logic styles are difficult to achieve. However, the performance enhancement comes with several costs, including reduced noise margin, charge-sharing noise, and higher power dissipation due to higher data activity. Because of dynamic logic's limitations and diminished speed reward, a slowly rising need has emerged in the past decade to explore new logic style that goes beyond dynamic logic. To improve the performance of dynamic logic circuit in terms of speed and power, new logic family called feedthrough logic was proposed in [4], where FTL concept is extended for the design of low power and high performance arithmetic circuits. This logic works on domino concept along with the important feature that output is partially evaluated before all the inputs are valid. This feature results in very fast evaluation in computational block. In this paper, the proposed design of a low power FTL circuit that further improves the power consumption of FTL.

The total power dissipated in a generic CMOS digital gate is given by

$$P_{total} = P_{static} + P_{dynamic} + P_{short\ circuit}$$
$$= V_{dd} I_i + V_{dd} F_{clk} \Sigma V_{i\ swing} C_{i\ load} \alpha_i + V_{dd} \Sigma I_{i\ sc}$$

Where $V_{i\ swing}$ is the voltage swing, $C_{i\ load}$ is the load capacitance, α_i the switching factor, $I_{i\ sc}$ is the short circuit current and I_I is the leakage current at node i respectively and F_{clk} denotes the system clock frequency.

II. PRINCIPLE OF CONVENTIONAL FTL

FTL logic [Fig.1 (b)] in CMOS technology was first introduced in [4] and [5]. Its basic operation is as follows: when CLK is high, the pre-discharge period begins and Out is pulled down to GND through M2. When CLK becomes low, M1 is on, M2 is off, and the gate enters the evaluation period. If inputs (IN) are logic "1," Out enters the contention mode where M1 and transistors in the NMOS PDN are conducting current simultaneously. If PDN is off, then the output quickly rises to logic "1."

- It only requires NMOS transistor logic expression
- The critical path is constant regardless of the logic expression

- The output is pre-evaluated before the inputs from the preceding stage is ready

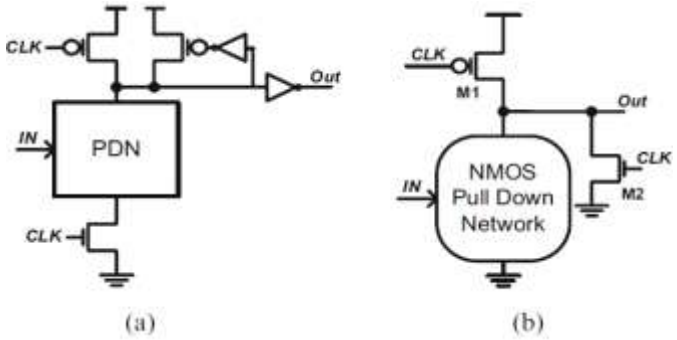

Fig.1 (a) Dynamic Domino Logic (b) FTL

Despite its performance advantage, FTL suffers from reduced noise margin, excess direct path current, and nonzero nominal low output voltage, which are all caused by the contention between M1 and NMOS PDN during the evaluation period. Furthermore, cascading multiple FTL stages together to perform complicated logic evaluations is not practical. Consider a chain of inverters implemented in FTL cascaded together and driven by the same clock. When CLK is low, M1 of every stage turns on, and the output of every stage begins to rise. This will result in false logic evaluations at even numbered stages since initially there is no contention between M1 and NMOS PDN because all inputs to NMOS transistors are reset to logic "0" during the reset period.

Existing FTL Techniques

1. LP-FTL

The low power FTL circuit is shown in Figure 2 (a). This circuit reduces VOL by using one additional PMOS transistor MP2 in series with MP1. The operation of this circuit is similar to that of FTL. During reset phase i.e. when CLK = 1, output node is pulled to ground (GND) through Mr. During evaluation phase output node charges through Mp1 and Mp2. When CLK goes low (evaluation phase) Mr is turned off and the output node conditionally evaluates to logic high (VOH) or low (VOL) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward VDD i.e. VOH =VDD, otherwise it remain at logic low i.e. VOL. Since Mp1 and Mp2 are in series the voltage at drain of MP1 is less than VDD. During evaluation due to ratio logic the output node pulled to logic low voltage i.e. VOL which is less than the VOL of existing FTL. This reduction in VOL causes significant reduction in dynamic power consumption but due to the insertion of PMOS transistor Mp2 propagation delay of the LP-FTL increases.

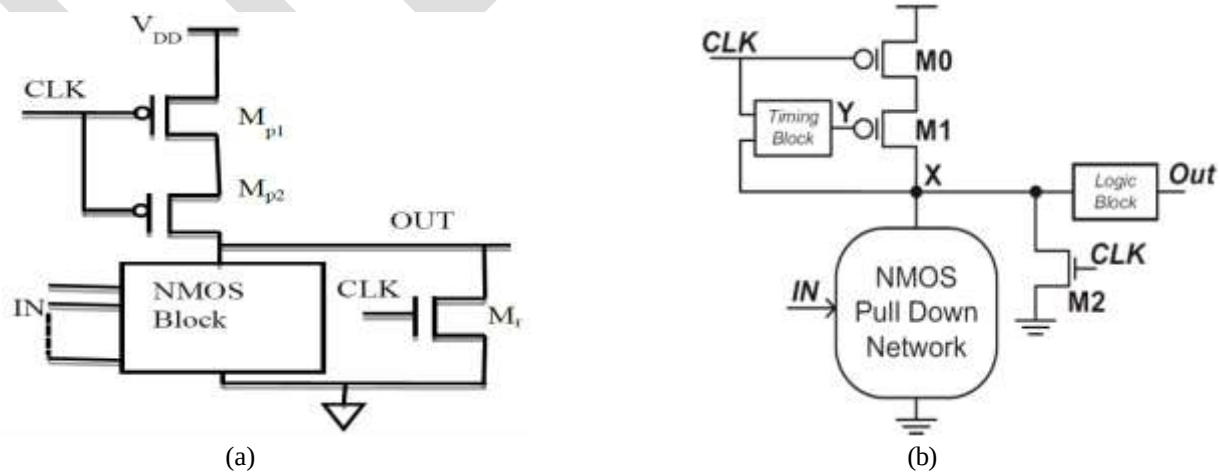

Fig.2 (a) Low Power Feedthrough Logic (LP-FTL), (b) Constant Delay Logic(CD Logic)

2. CD Logic

To mitigate the contention problems, CD logic is proposed with a schematic shown in Figure 2 (b). Timing block (TB) creates an adjustable window period to reduce the static power dissipation. When CLK is high, CD logic predischarges both X and Y to GND. When CLK is low, CD logic enters the evaluation period and three scenarios can take place: namely, the contention, C–Q delay and D–Q delay modes. The contention mode happens when CLK is low while IN remains at logic "1". In this case, X is at a nonzero voltage level which causes Out to experience a temporary glitch. The duration of this glitch is determined by the local window width, which is determined by the delay between CLK and CLK_d. When CLK_d becomes high, and if X remains low, then Y rises to logic "1", and turns off M1. Thus the contention period is over, and the temporary glitch at Out is eliminated.

C–Q delay mode takes places when IN make a transition from high to low before CLK becomes low. When CLK becomes low, X rises to logic "1" and Y remains at logic "0" for the entire evaluation cycle. D–Q delay mode utilizes the pre-evaluated characteristic of CD logic to enable high-performance operations. In this mode, CLK falls from high to low before IN transit, hence X initially rises to a nonzero voltage level. As soon as IN become logic "0", while Y is still low, then X quickly rises to logic "1". If CLK_d rises slightly slower than X, then Y will initially rise (thus slightly turns off M1) but eventually settle back to logic "0". CD logic can still perform the correct logic operation in this case, however, its performance is degraded because of M1's reduced current drivability. The CD logic reduce short circuit power dissipation which occur in contention period but it also suffer from additional transistors overhead and the need of adjust the window size depending upon environment.

PROPOSED ENERGY-EFFICIENT FEEDTHROUGH LOGIC

The proposed EE-FTL circuit is shown in Figure 3. This circuit consists of additional PMOS pull up transistor (T3) in series with T1. The T3 transistor is controlled by the drain signal of T2 transistor. The inverted clock signal is given to source of T2. The output signal is taken to control gate terminal of T2. T4 transistor is connected to reset the node X, when CLK is high. T6 transistor is used to reset the output terminal. The single bit input signal is given to pull down NMOS transistor T5. There are two modes of operation in EE-FTL circuit namely, reset mode and evaluation mode. When CLK is high, both X and OUT pre-discharges to GND. Thus the output of EE-FTL circuit is always at logic "0" when CLK is high. So it is called as reset mode.

When CLK is low, circuit enters the evaluation mode and the contention mode take place. In the contention mode, CLK is low while input (IN) at logic "1". In this case, both PUN and PDN will simultaneously conduct, which causes a temporary glitch at output node. This will create direct path exist between power supply and ground. The power dissipation occurs due to this short circuit current is known as short circuit power dissipation. This effect can be reducing by EE-FTL circuit. The output node become a non zero voltage level at this mode. This voltage level is used to turn on the transistor T2 by feedback method. The high level inverted clock signal pass through T2 and disables the T3 transistor. Thus the direct path is disabled till the entire contention period and the glitches also eliminated.

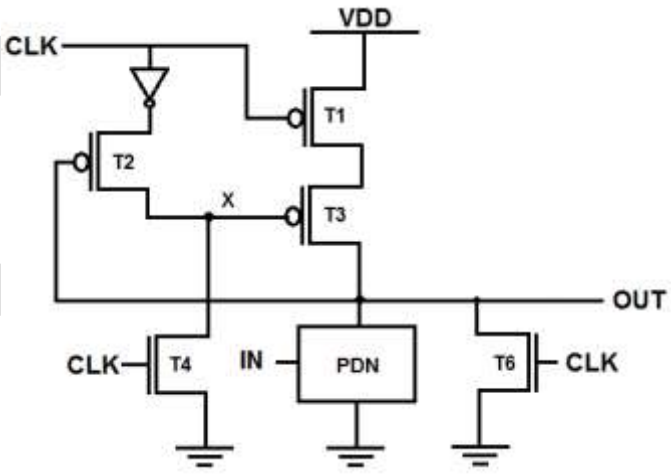

Fig.3 ENERGY-EFFICIENT FEEDTHROUGH LOGIC (EE-FTL)

Design of Full Adder Using EE-FTL Technique

A one bit CMOS full adder is designed using EE-FTL technique is shown in figure 4. The carry generation circuit and sum generation circuit is configured by EE-FTL. Since the output of FTL is inverted, two inverters is used at the end of both sum and carry section. Common clock signal is used in the entire circuit. The inputs which are in series at sum generation circuit will increase the parasitic effects, when both inputs A and B are at logic "1" and carry input is logic"0". But EE-FTL circuit will not be affected by this condition.

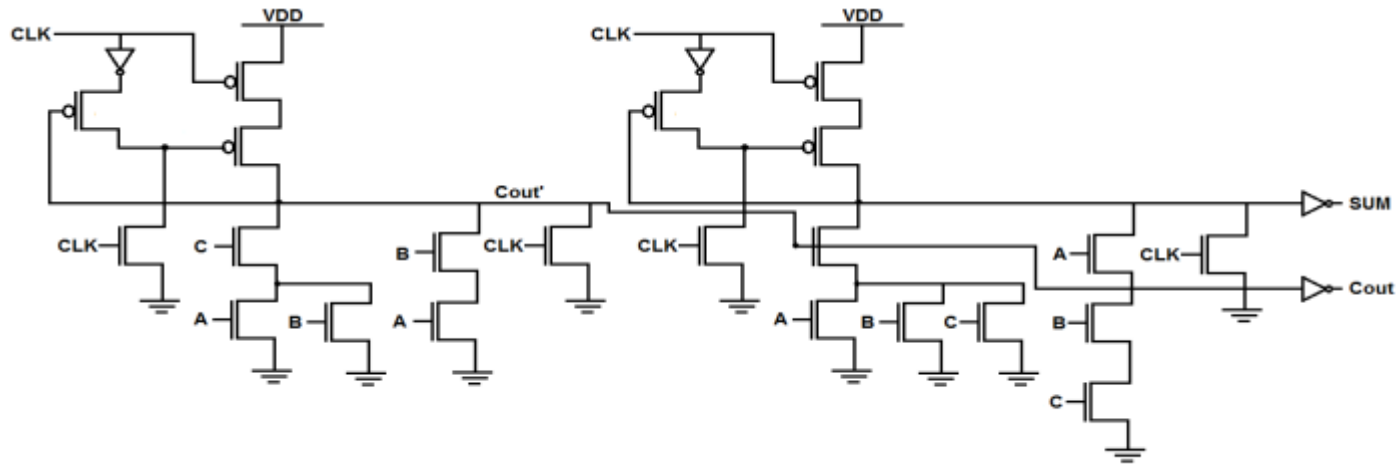

Fig.4 CMOS Full Adder using EE-FTL technique

SIMULATION RESULT AND DISCUSSION

The full adder is designed using several techniques styles such as LP-FTL, MFTL, CDL and EE-FTL. These adders are designed using MICROWIND DSCH2 tool. The several parameters such as power, area and delay are obtained from simulation results. Figure 5 shows the simulated waveform of full adder circuit using EE-FTL. Table 1 shows the comparison of several parameters. The area overhead of EE-FTL is less compare to CD logic but high when compare to FTL, LP-FTL techniques. The EE-FTL technique has less speed than the other techniques which is tolerable when power is main concern compare to delay. While EE-FTL require more area compare to FTL, EE-FTL is still an attractive choice in a high-performance full-custom design because of very less power consumption. Figure 6 shows the bar chart of data in comparison table. The overall comparison makes the EE-FTL is more suitable for low power arithmetic circuits.

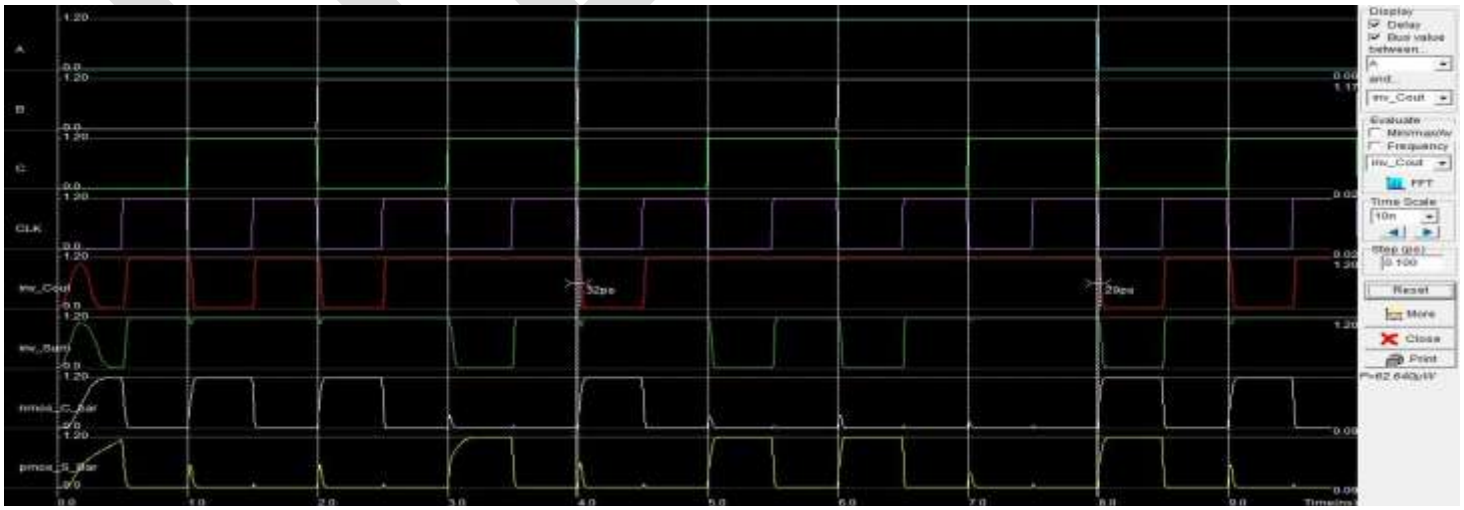

Fig.5 Simulated Waveform of Full Adder Using EE-FTL

Table 1 Comparison Table of one bit full adder using EE-FTL

Logic Style	Area (μm^2)	Power (μW)	Delay (ps)	Power Delay Product(PDP) (fJ)	Energy Delay Product(EDP) (fJ.ps)
FTL	177.9	273	18	4.914	88.452
LP-FTL	207.3	211	25	5.275	131.875
CDL	389.7	98.62	28	2.761	77.308
EE-FTL	303.6	62.64	29	1.816	52.664

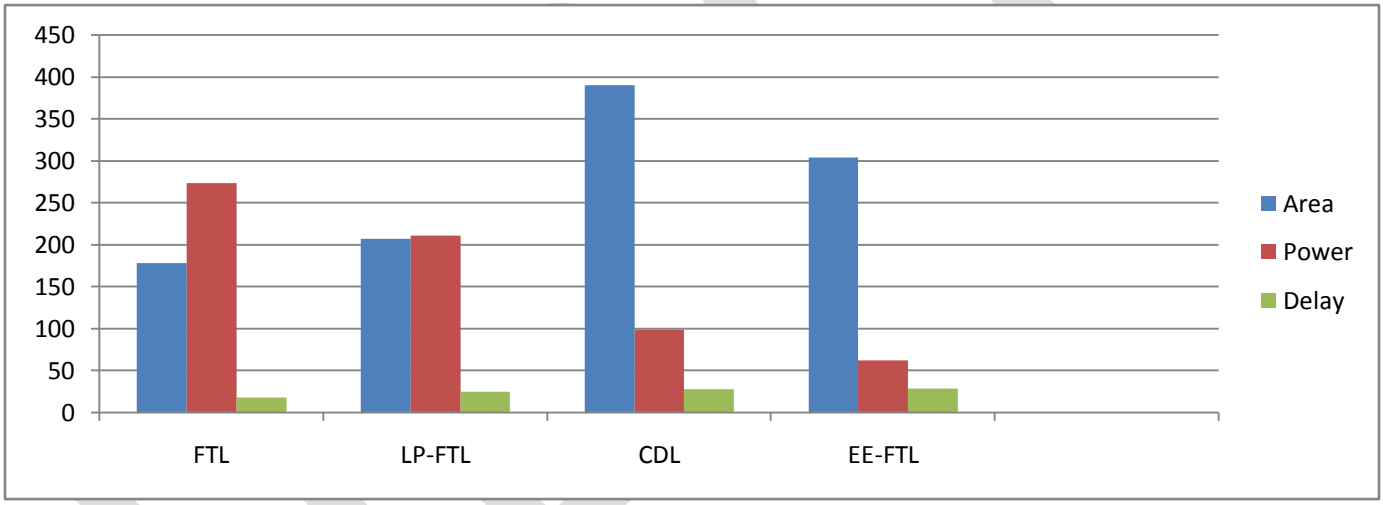

Fig.6 Bar Chart of One Bit Full Adder parameters

CONCLUSION

A new energy efficient feedthrough logic was proposed in this paper to reduce short circuit power dissipation in contention mode. The pre-evaluated feature of EE-FTL makes it particularly suitable in a circuit block where performance is the primary concern. The proposed logic style requires low power when compare to the existing feedthrough logic. The proposed circuit is simulated and a comparison analysis has been carried out using 90 nm, 1.2V CMOS process technology. A CMOS Full Adder is designed by EE-FTL techniques and the simulation result in MicroWind environment shows that the proposed logic reduces the power consumption by 77%, 70% and 36% over FTL, LP-FTL and CDL, respectively. The simulation result confirms that at same frequency of operation the power delay product of proposed circuits is much better than that of existing FTL structure.

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