

Analysis and Control of Three Phase Multi level Inverters with Sinusoidal PWM Feeding Balanced Loads Using MATLAB

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Abstract— Multi level inverters are becoming very attractive for industries due to their high power rating, high voltage rating and high efficiency is achieved without transformer. These also improves the overall performance of the system as these produces fewer harmonics. As the number of levels increases the quality of voltage waveform is also increases. In this paper the analysis of Three Phase Diode Clamped Multi Level Inverter has been carried out in MATLAB/Simulink for different levels (3, 5 and 7) at varying loads. Diode-Clamped topology for Multi level inverter (DC-MLI) for different levels are analyzed in the terms of THD contents for output voltage and as well in output current. Sinusoidal PWM Technique is used to generate the gate pulses. The simulation of three phase three level, five level and seven level inverters is done in Matlab/Simulink.

I. INTRODUCTION

In multilevel inverters the main dc supply voltage is divided into several smaller sources which are further used to synthesize an ac voltage source into a staircase or stepped approximation of the desired sinusoidal waveform. The multilevel inverters combine the individual dc sources at particular times to make a sine wave. And by using more levels to synthesize the sine waveform, the waveform approaches the desired sine and the total THD is reduced to nearly zero.

Types of Multi level inverters

Mainly three types of Multi level inverters are there:

- Diode-Clamped inverter
- Flying Capacitor inverter
- Cascaded inverter

In this paper Diode-Clamped topology for Multi level inverter [10] is used. The simplest form of this topology is also known as the neutral point clamped converter. In this there are two pairs of switches (upper and lower).

For an 'M- level' Diode Clamped-Multi-Level Inverter:-

No. of Power Semi-Conductor Switches per phase = $2(m-1)$

Clamping diodes per phase = $(m-1)(m-2)$

DC bus capacitors = $(m-1)$

Where m = No. of levels

The main role of capacitors is to divide the main dc voltage into smaller voltages i.e. for five level it is V_{dc} , $\frac{1}{2} V_{dc}$, 0 , $-\frac{1}{2} V_{dc}$ and $-V_{dc}$.

Diode-Clamped topology for Multi level inverter (DC-MLI) has a number of advantages some of them are as follows:

- The THD decreases with the increase in number of level.
- Common DC bus is used for all the phases.
- Flow of Reactive power can be controlled.

- Control scheme is quite simple.

II. MODULATION TECHNIQUE

The control of Multi level Inverter is much complicated as compared to two level Voltage source Inverter because extra need for the timing transitions between the voltage levels. Sinusoidal PWM, Space Vector Modulation and Harmonics Elimination PWM are some of the main modulation techniques for Multi level Inverter but Sinusoidal PWM is found the most popular method. The Space Vector Modulation and Harmonics Elimination PWM are used for some specific applications.

In Sinusoidal PWM, comparison of Reference (Sine) with Triangular waves (N-1) are done. The resulting intersection points are used as the switching instants of PWM pulses as shown in Figure 1.

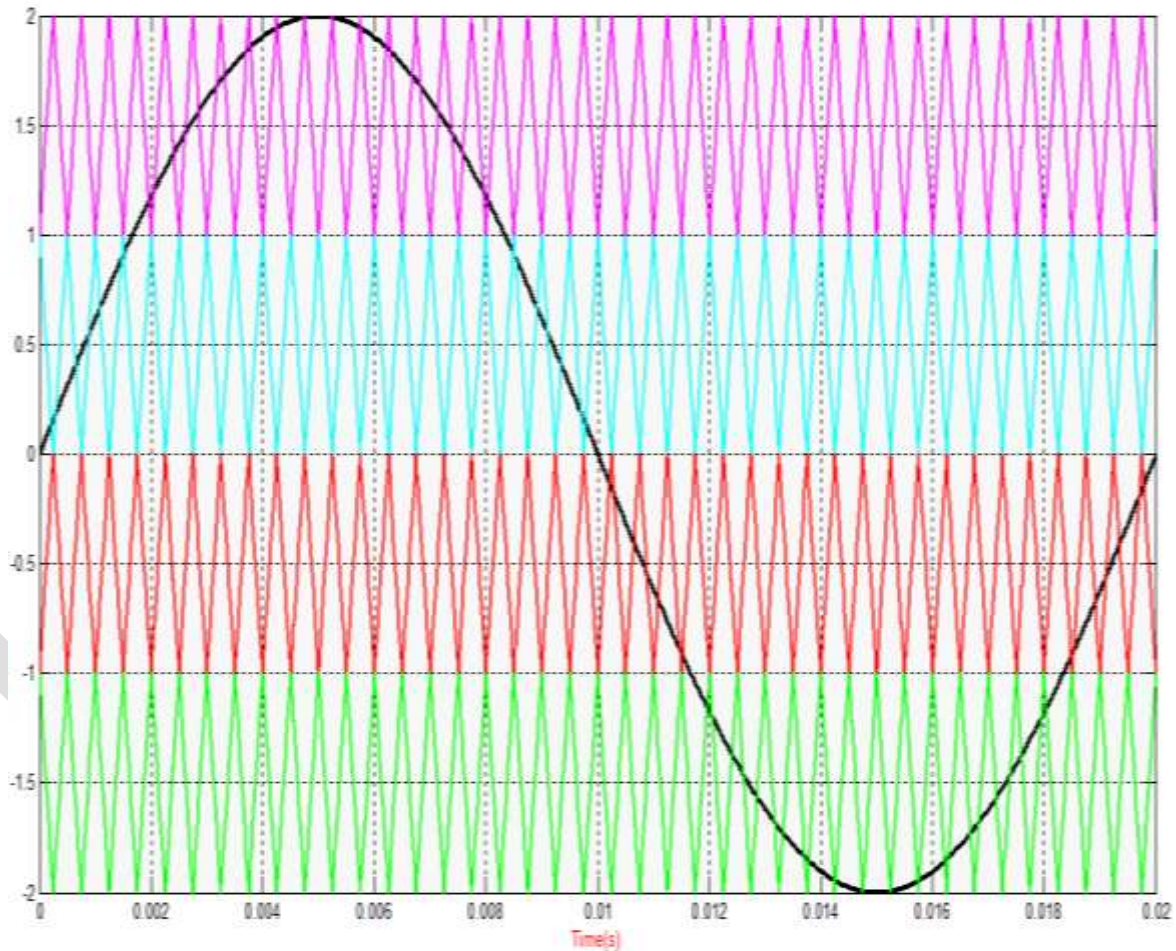


Figure 1 Comparison of Triangular Waves with Sine Wave

III. MATLAB SIMULATION

The main objective of this paper is to generate the gate pulses for the thyristors used in the Diode-Clamped Inverter. The gate pulses are generated by the SPWM method. When we compare the two waves i.e. Sine and Triangular, the pulses are generated which are further used to control the VSI. Matlab Simulation of 5- Level Diode-Clamped Inverter is shown in figure 2

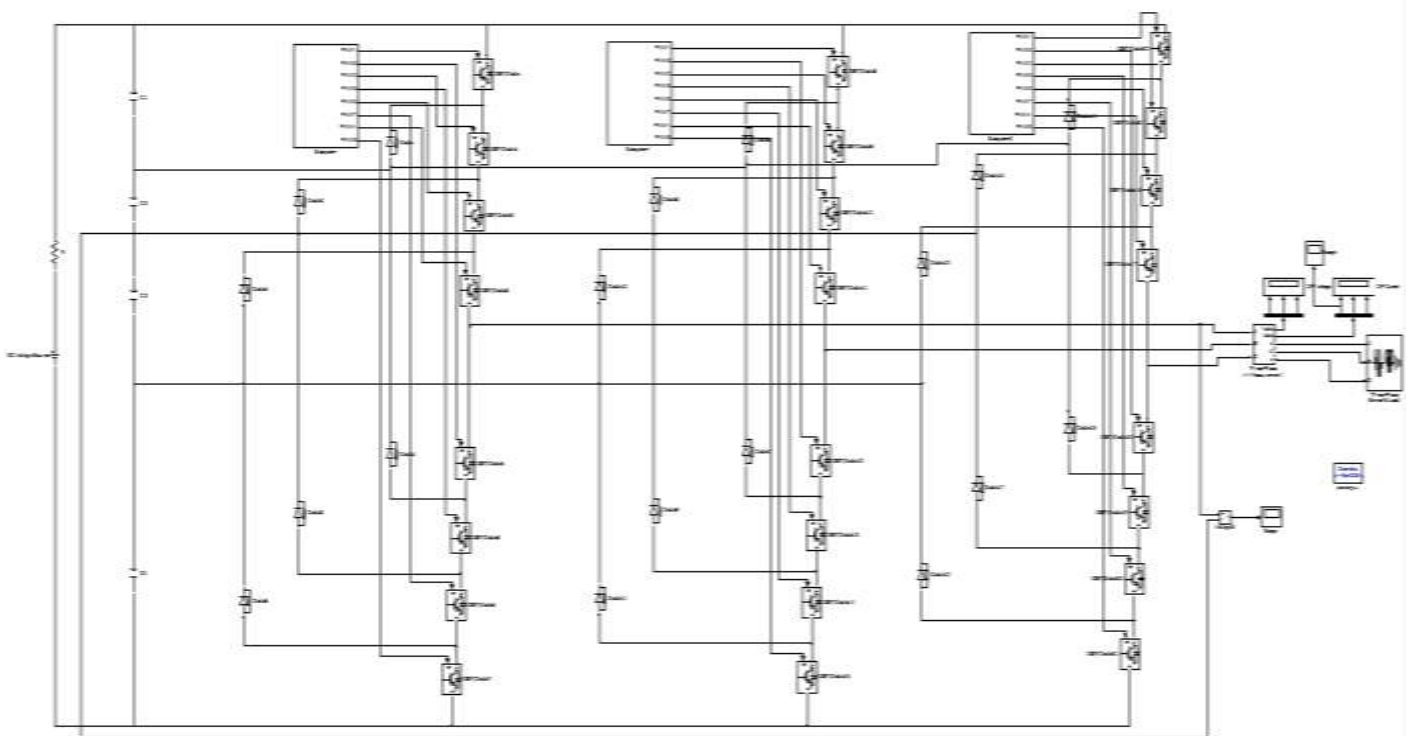


Figure 2 Matlab Simulation of 5- Level Diode-Clamped Inverter

IV. SIMULATION RESULTS

Different Level Inverters are analyzed for different values of loads. R-L load is taken for all the outputs and the power factor is taken as 0.8.

A. Output Phase Voltage of 3-Level Inverter

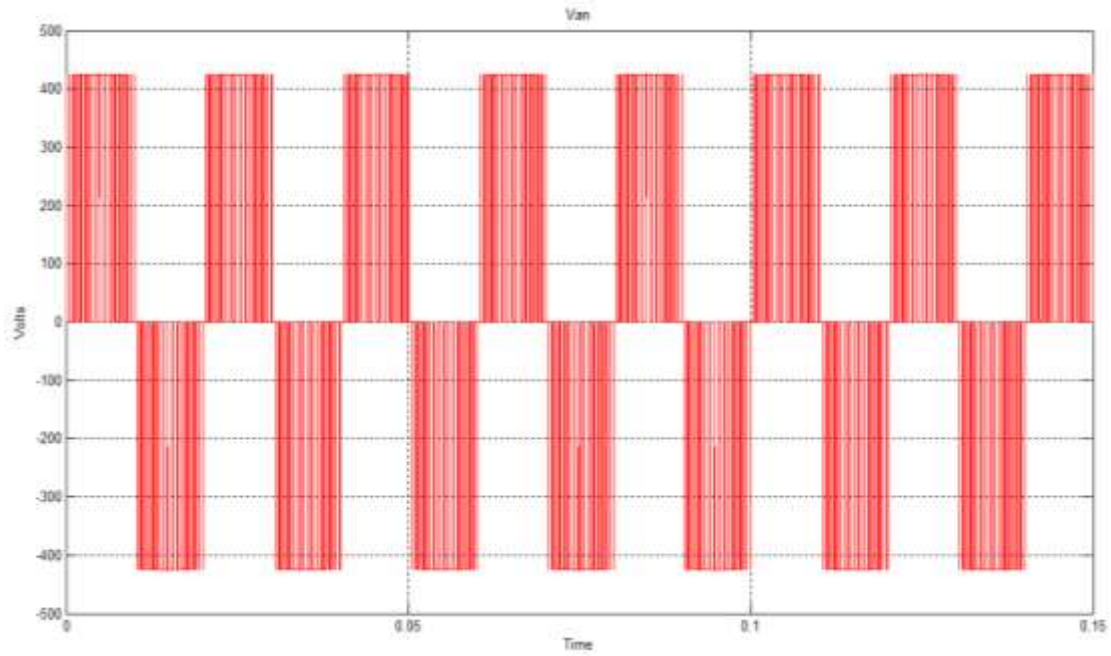


Figure 3. Output Phase Voltage of 3-Level Inverter

B. Output Current of 3-Level Inverter at 1 KW

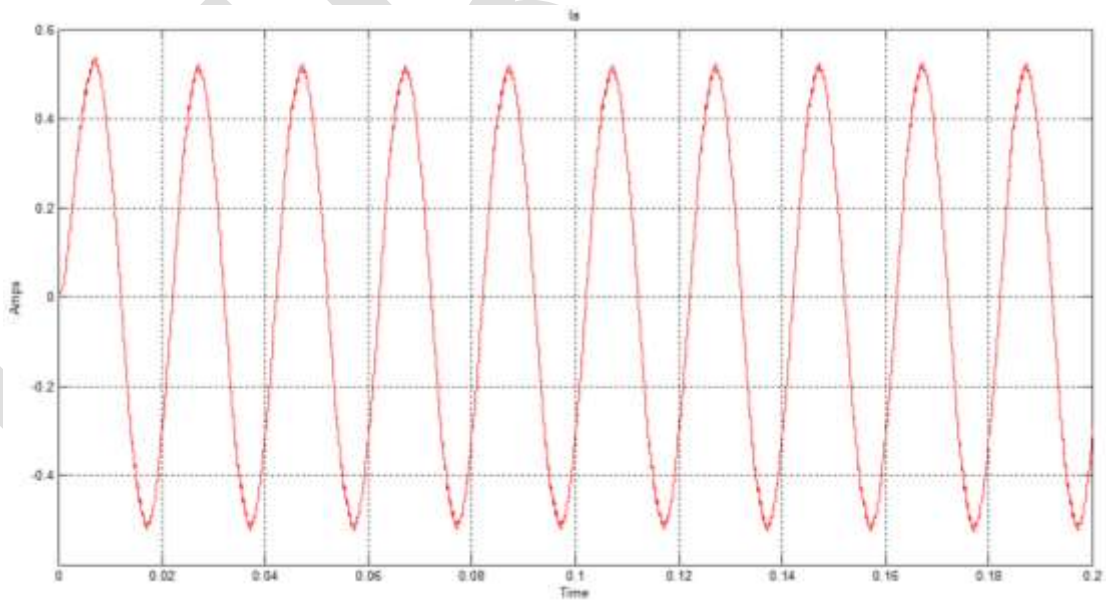


Figure 4. Output Current of 3-Level Inverter at 1 KW

C. Output Phase Voltage of 5-Level Inverter

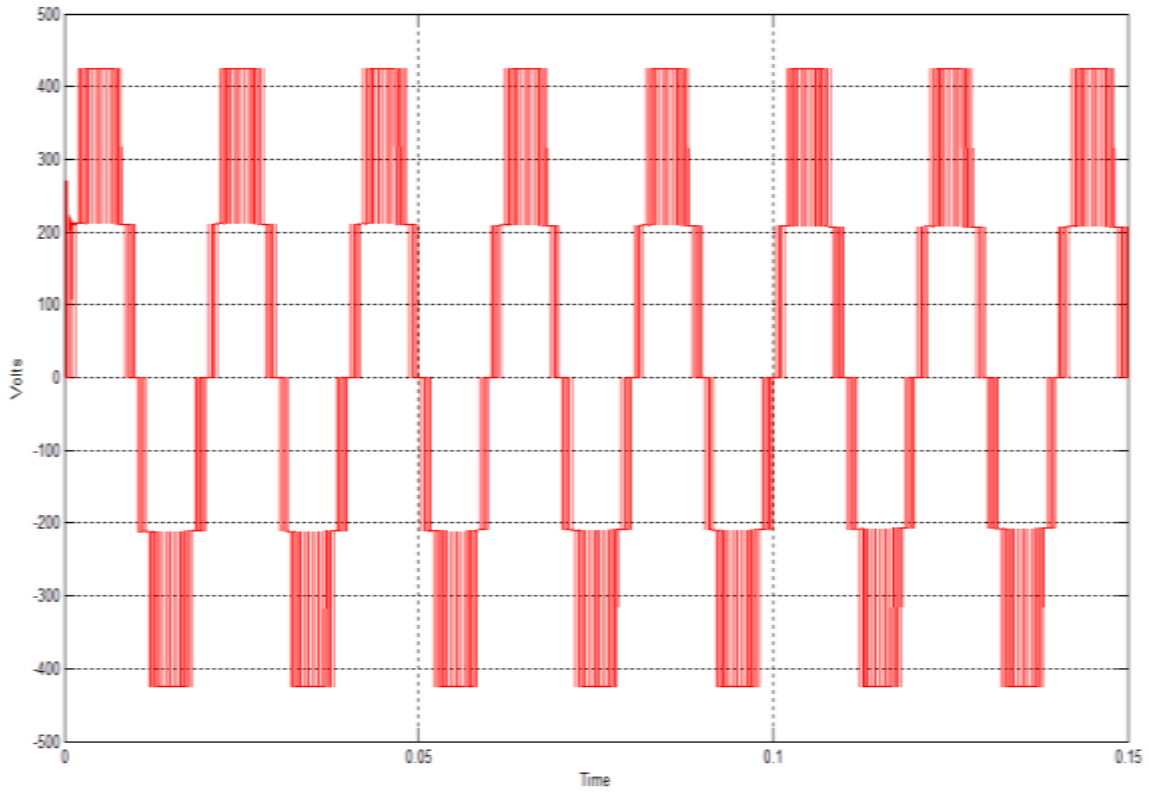


Figure 5. Output Phase Voltage of 5-Level Inverter

D. Output Current of 5-Level Inverter at 1 KW

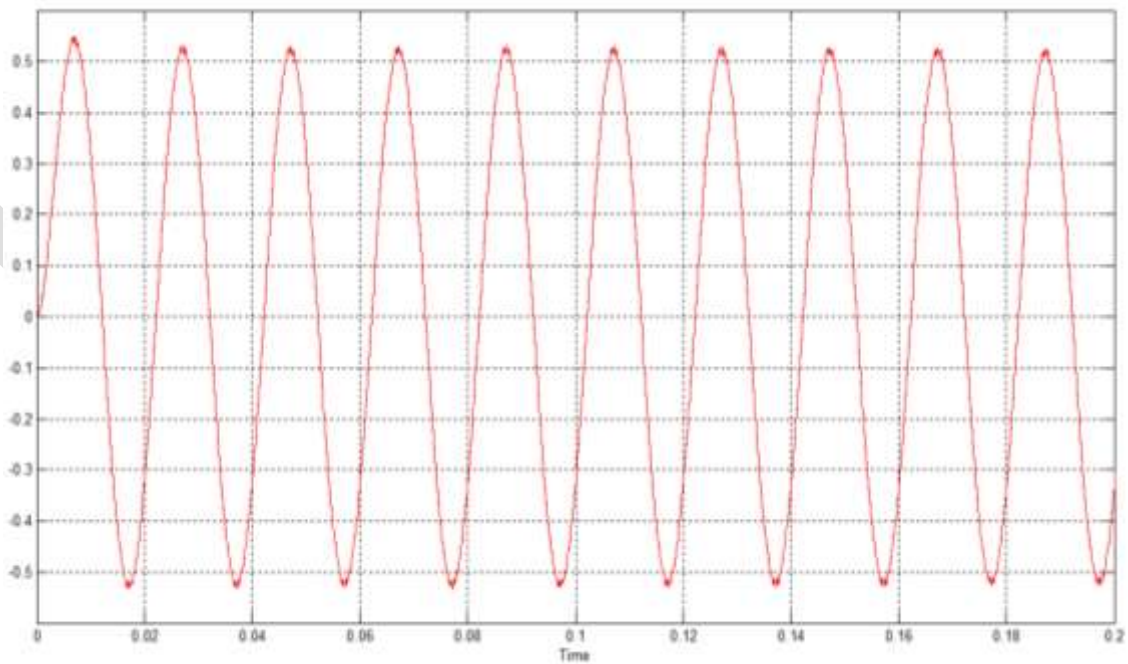


Figure 6. Output Current of 5-Level Inverter at 1 KW

E. Output Phase Voltage of 7-Level Inverter

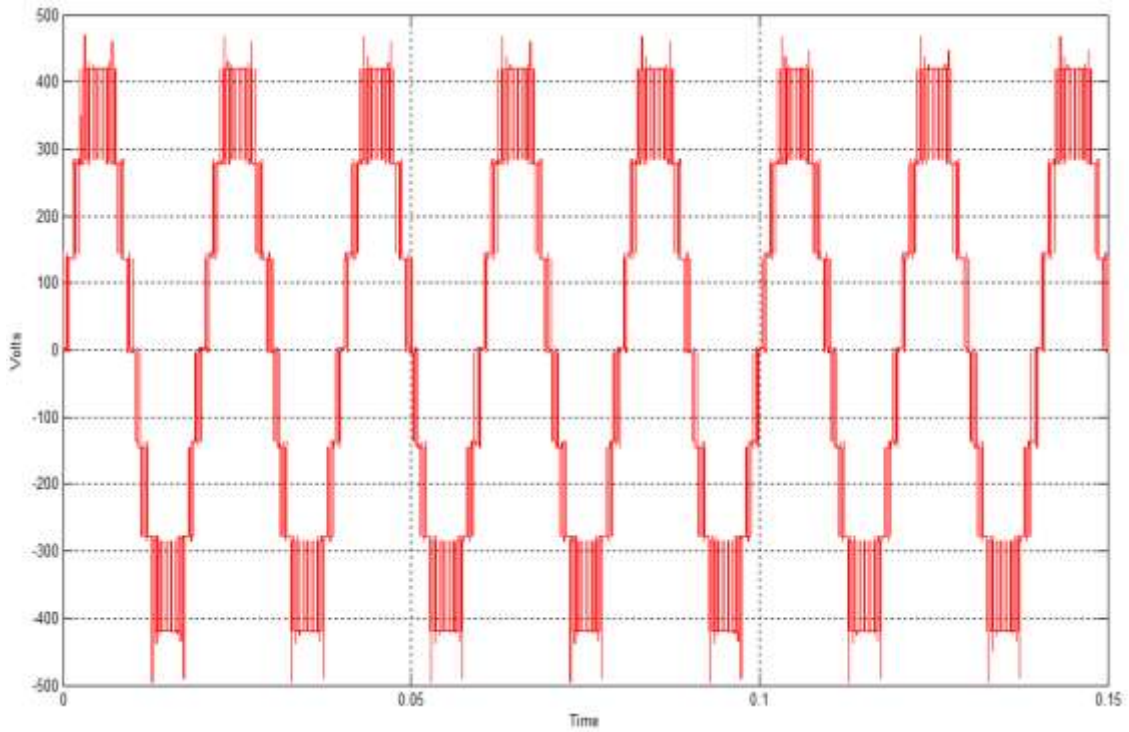


Figure 7. Output Phase Voltage of 7-Level Inverter

F. Output Current of 7-Level Inverter at 1 KW

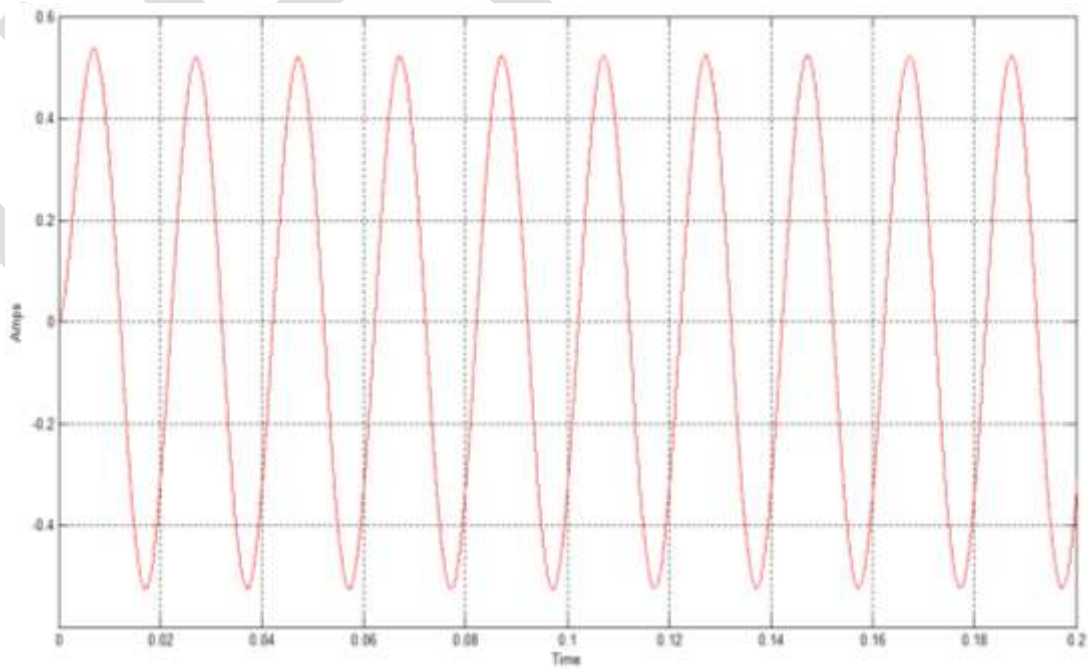


Figure 8. Output Current of 7-Level Inverter at 1 KW

V. RESULTS

The THD for output voltages and output currents is summarized in the tables. Table 1 shows the comparison of the THD of Output Currents of different Levels at different loads. And Table 2 shows the comparison of the THD of Output Voltages of different Levels at different loads.

Table No.1

Load		1 KW	3 KW	5 KW	7 KW	9 KW
Level						
3-Level Inverter	Current	0.5115	1.534	2.556	3.578	4.6
	THD	1.99 %	1.99 %	1.99 %	1.99 %	1.99 %
5-Level Inverter	Current	0.5214	1.534	2.509	3.447	4.348
	THD	1.14 %	1.26 %	1.40 %	1.56 %	1.73 %
7-Level Inverter	Current	0.5227	1.563	2.602	3.641	4.678
	THD	0.55 %	0.55 %	0.54 %	0.53 %	0.53 %

Table No.2

Load		1 KW	3 KW	5 KW	7 KW	9 KW
Level						
3-Level Inverter	Voltage	410.8	410.6	410.5	410.5	410.4
	THD	57.19 %	57.27 %	57.27 %	57.27 %	57.26 %
5-Level Inverter	Voltage	417.7	409.5	401.5	393.8	386.34
	THD	28.12 %	29.69 %	31.57 %	33.74 %	36.22 %
7-Level Inverter	Voltage	418.5	417.2	416.7	416.4	416.2
	THD	18.80 %	19.41 %	19.52 %	19.54 %	19.55 %

VI. CONCLUSION

This paper has evaluated the Sinusoidal PWM technique for Diode-Clamped Multi level. In this paper, Simulink model for same has been developed and tested in the MATLAB/Simulink environment for different values of Loads. The simulation results are compared and analyzed by plotting the output harmonic spectra of various output Currents and output Voltages and computing their Total Harmonic Distortion (THD) and their final comparison is shown in Tables. It is observed that with the increase of level the THD of output current and voltage decreases. THD of load currents at all levels is less than 5 % shows the durability of design of this multilevel inverter. It is clear from the comparison that the Harmonics are reduced as the number of Levels increases and hence the overall system efficiency increases.

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